PULSE AND DIGITAL CIRCUITS (EC402ES)

II-B.Tech II- Sem-ECE

(R16 Regulation)

Prepared by

MD.GANDHI BABU

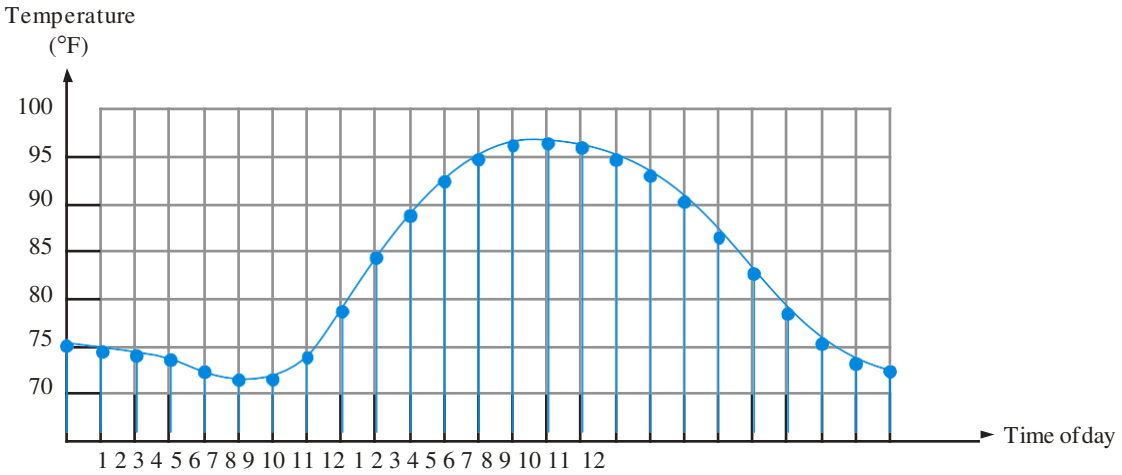
UNIT-1

LINEAR WAVESHAPING

Basics

Analog Quantities

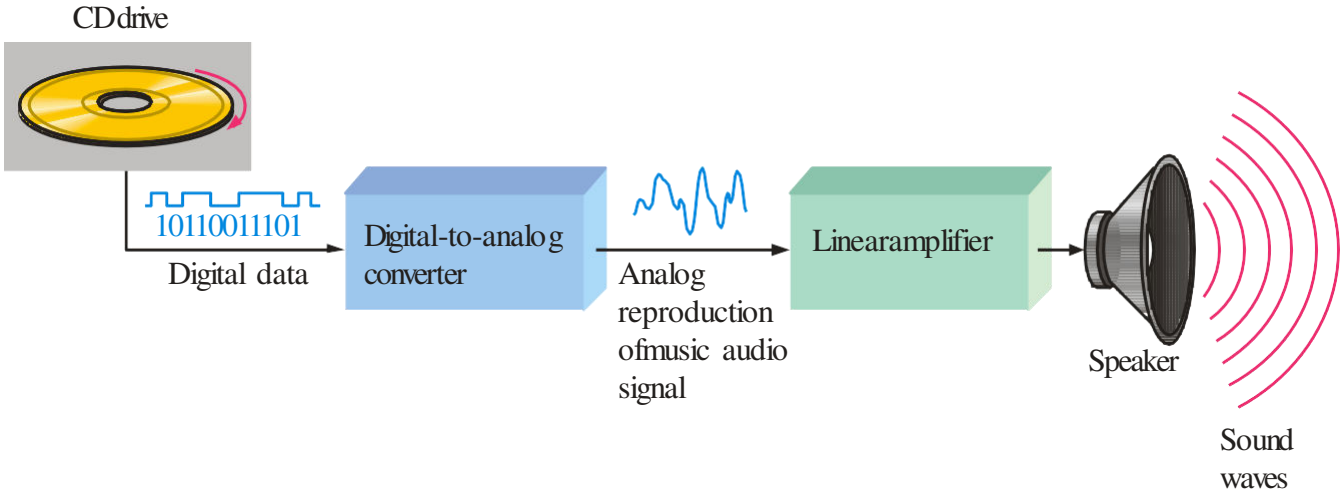
- Most natural quantities that we see are **analog** and vary continuously. Analog systems can generally handle higher power than digital systems



- Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point

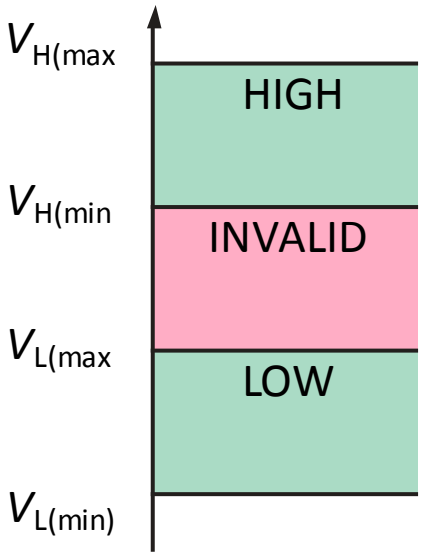
Analog and Digital Systems

- Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point



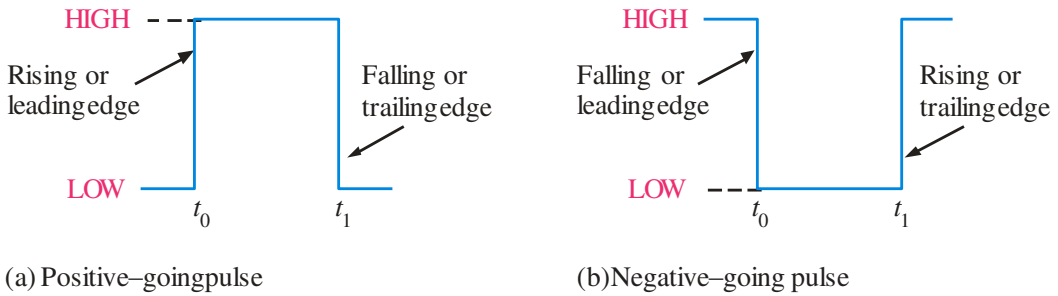
Contd..

- Digital electronics uses circuits that have two states, which are represented by two different voltage levels called HIGH and LOW. The voltages represent numbers in the binary system
- In binary, a single number is called a *bit* (for *b*inary dig*it*). A bit can have the value of either a 0 or a 1, depending on if the voltage is HIGH or LOW.



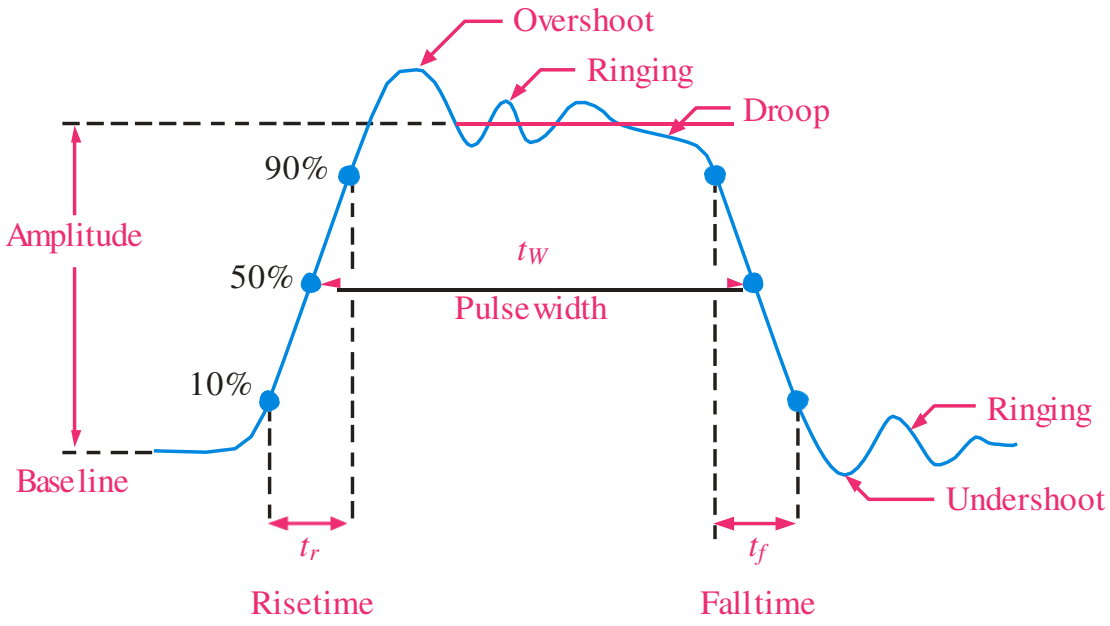
Digital Signals

- Digital waveforms change between the LOW and HIGH levels. A positive going pulse is one that goes from anormally LOW logic level to a HIGH level and then back again. Digital waveforms are made up of a series of pulses



Pulse Definitions

- Actual pulses are not ideal but are described by the rise time, fall time, amplitude, and other characteristics.



Periodic Pulse Waveforms

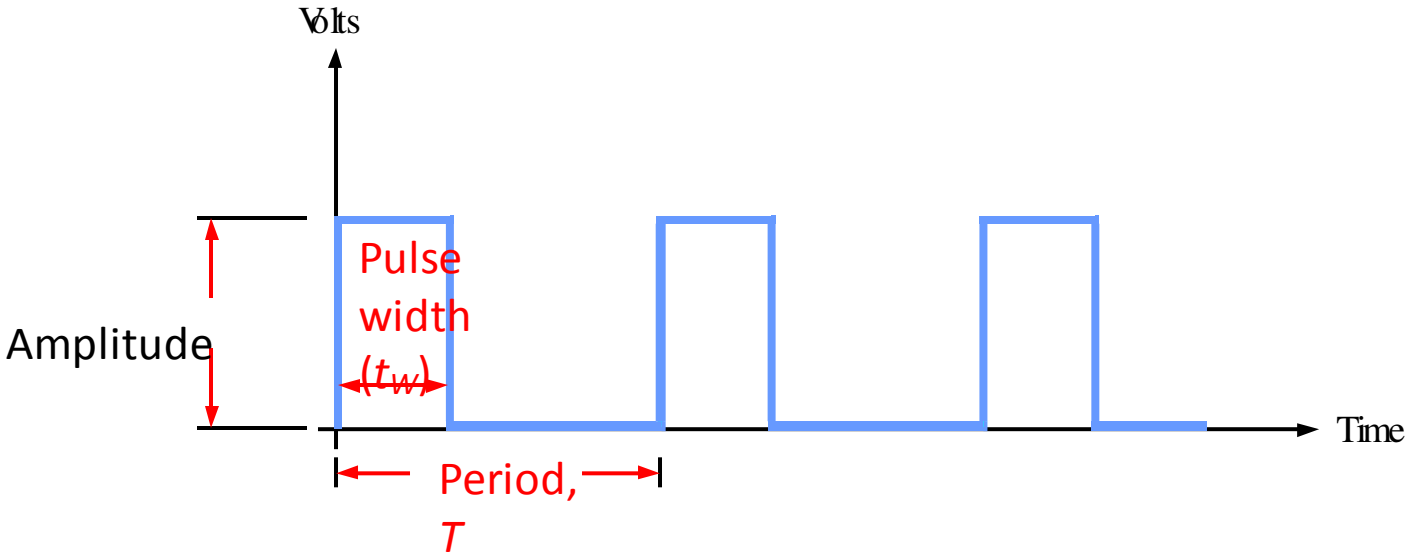
- Periodic pulse waveforms are composed of pulses that repeats in a fixed interval called the **period**.
- The **frequency** is the rate it repeats and is measured in hertz. The **clock** is a basic timing signal that is an example of a periodic wave.
-

$$T = \frac{1}{f} z$$

What is the period of a repetitive wave if $f = 3.2\,\text{GHz}$?

Pulse Definitions

- In addition to frequency and period, repetitive pulse waveforms are described by the amplitude (A), pulse width (t_W) and duty cycle. Duty cycle is the ratio of t_W to T.



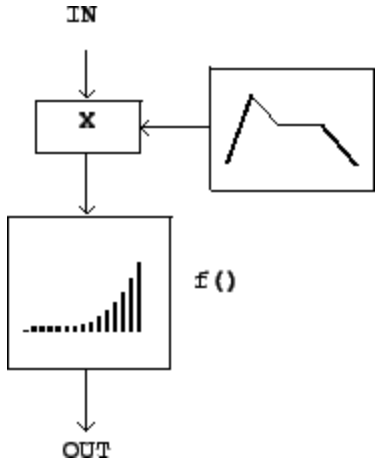
Wave Shaping

Definition: It is the process of changing the shape of input signal with linear / non-linear circuits.

Types:

i. Linear Wave Shaping

ii. Non-linear Wave Shaping



Linear Wave Shaping

Definition: The process where by the form of a non-sinusoidal signal is changed by transmission through a linear network is called Linear Wave Shaping.

Types:

i. High Pass RC Circuit.

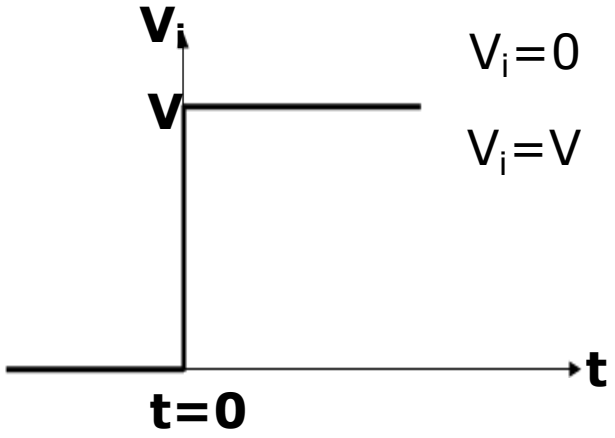
ii. Low Pass RC Circuit.

Non-sinusoidal wave forms

1) Step
2) Pulse
3) Square wave
4) Ramp
5) Exponential wave forms.

Step Waveform

A step voltage is one which maintains the value zero for all times t<0 and maintains the value V for all times t>0.

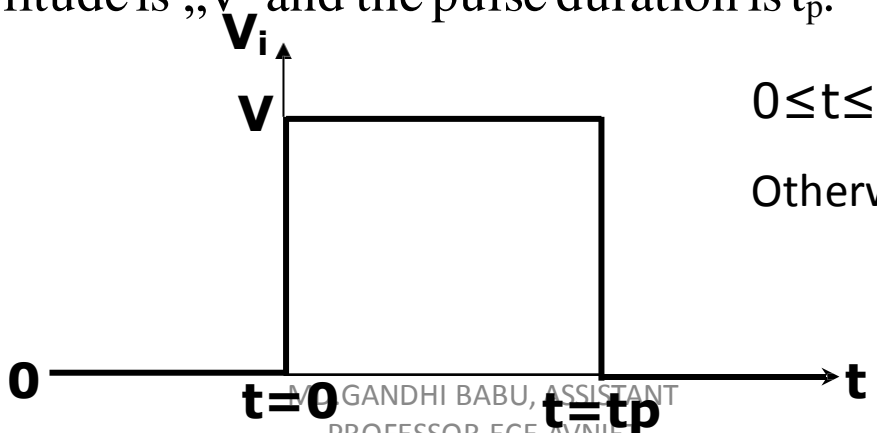


$V_i = 0 \quad t < 0$

$V_i = V \quad t > 0$

Pulse

The pulse amplitude is „V" and the pulse duration is t_p.

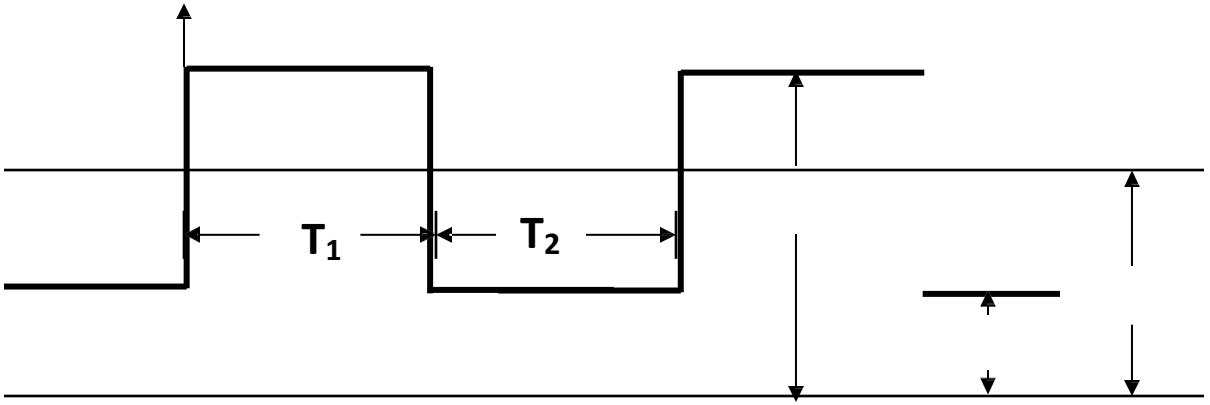


$0 \le t \le tp \quad V_i = V$

Otherwise $V_i = 0$

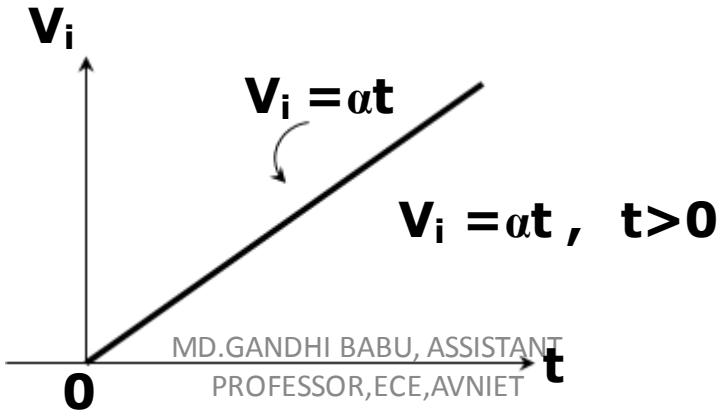
Square Wave

- A wave form which maintains itself at one constant level v^1 for a time T_1 and at other constant Level V^{11} for a time T_2 and which is repetitive with a period $T=T_1+T_2$ is called a square-wave.



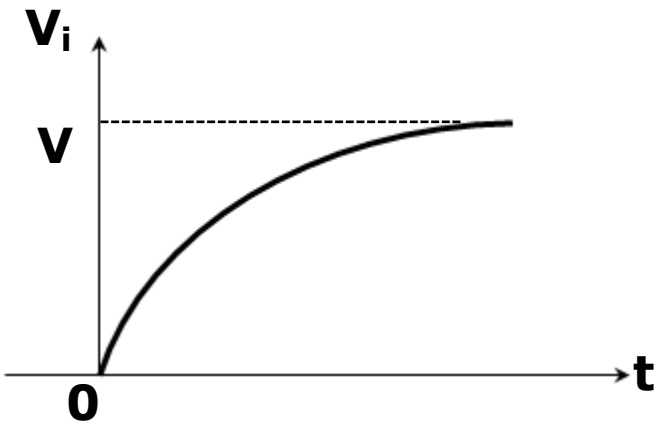
Ramp

A waveform which is zero for t<0 and which increases linearly with time for t>0.

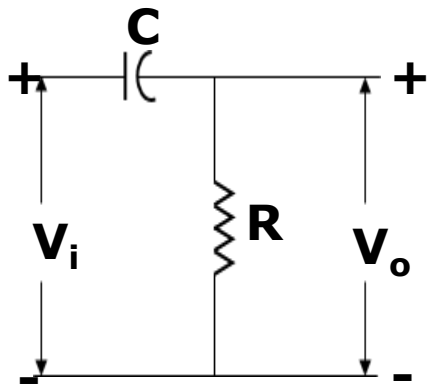


Exponential

- The exponential waveform input is given by where T is the time constant of the exponential input



High Pass RC Circuit



$$X_C = \frac{1}{2\Pi fC}$$

If f=low, X_c becomes high

C act as open circuit, so the V_o=0.

If f=high, X_c becomes low

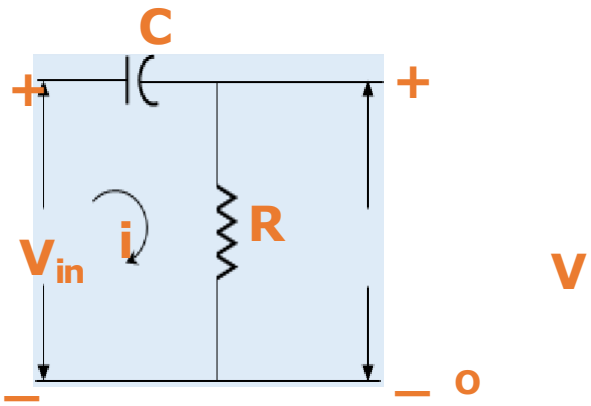
C acts as short circuit, so we get the output.

The higher frequency components in the input signal appear at the output with less attenuation due to this behavior the circuit is called "High Pass Filter".

Sinusoidal input

- For Sinusoidal input, the output increases in amplitude with increasing frequency.

$$V_o = iR$$



$$i = \frac{V_{in}}{R - jX_C} = \frac{V_{in}}{R - \frac{j}{2\pi f C}}$$

$$i = \frac{V_{in}}{R\left[1 - \frac{j}{2\pi fRC}\right]}$$

$$V_O = iR = \frac{V_{in} \times R}{R\left[1 - \frac{j}{2\pi fRC}\right]} = \frac{V_{in}}{1 - \frac{j}{2\pi fRC}}$$

$$V_0 = \frac{V_{in}}{1 - j\frac{f_1}{f}} \quad \text{where } f_1 = \frac{1}{2\pi RC}$$

$$\frac{V_O}{V_{in}} = \frac{1}{1 + j\left(-\frac{f1}{f}\right)}$$

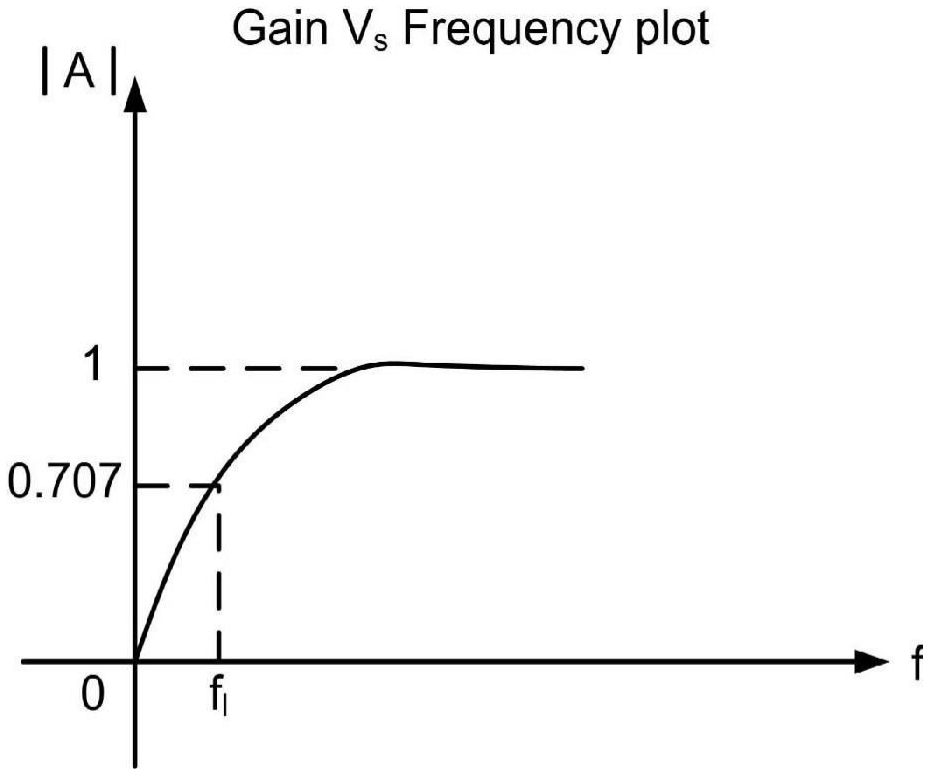
$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1 + \left|\left(\frac{f_1}{f}\right)\right|^2}}$$

$$|A| = 0.707$$

$$\theta = -\tan^{-1}\left|\left(\frac{-f_1}{f}\right)\right| = \tan^{-1}\left|\left(\frac{f_1}{f}\right)\right|$$

At the frequency $f = f_1$

$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707$$



At $f = f_1$ the gain is 0.707 or this level corresponds to a signal reduction of 3 decibels(dB).

$\therefore f_1$ is referred to as Lower 3-dB frequency.

Square wave input

- Percentage Tilt ($^0/_0$Tilt)

Tilt is defined as the decay in the amplitude of the output voltage wave due to the input voltage maintaining constant level

$$P = \frac{V_1 - V^1_{\ 1}}{V/2} X100$$

$$V_1' = V_1 . e^{-T_1/RC} \longrightarrow (1)$$

$$V_2' = V_2 . e^{-T_2/RC} \longrightarrow (2)$$

$$V_1' - V_2 = V \longrightarrow (3)$$

$$V_1 - V_2' = V \longrightarrow (4)$$

- A symmetrical square wave is one for which $T_1 = T_2 = T/2$ & because of symmetry $V_1 = -V_2$

By substituting these in above equation (3)

- $V_1' = -V_2'$

$$V = V_1' - V_2$$

$$V = V_1 . e^{-T/2RC} - V_2$$

$$V = V_1 . e^{-T/2RC} + V_1$$

$$V = V_1 (1 + e^{-T/2RC})$$

$$V_1 = \frac{V}{1 + e^{-T/2RC}} \longrightarrow \text{I}$$

Equation (1) $V_1' = V_1 . e^{-\frac{T}{2RC}}$

$$V_1' = \frac{V}{1 + e^{-T/2RC}} \times e^{-T/2RC} = \frac{V}{1 + e^{T/2RC}}$$

$$V_1' = \frac{V}{1 + e^{T/2RC}} \longrightarrow \text{II}$$

For $RC >> \frac{T}{2}$ the equation (I) & (II) becomes as

$$V_1 \cong \frac{V}{2}\left(1+\frac{T}{4RC}\right) \;\&\; V_1^1 \cong \frac{V}{2}\left(1-\frac{T}{4RC}\right)$$

The percentage tilt 'P' is defined by $P = \frac{V_1 - V_1^1}{V/2} \times 100$

$$P = \frac{\frac{V}{1+e^{-T/2RC}} - \frac{V}{1+e^{T/2RC}}}{V/2} \times 100$$

$$P = \left[\frac{1}{1+e^{-T/2RC}} - \frac{1}{1+e^{T/2RC}}\right] \times 200$$

$$P = \left[\frac{1}{1+e^{-T/2RC}} - \frac{e^{-T/2RC}}{1+e^{T/2RC}}\right] \times 200$$

$$P = \frac{1-e^{-T/2RC}}{1+e^{-T/2RC}} \times 200\%$$

High Pass RC circuit acts as differentiator:-

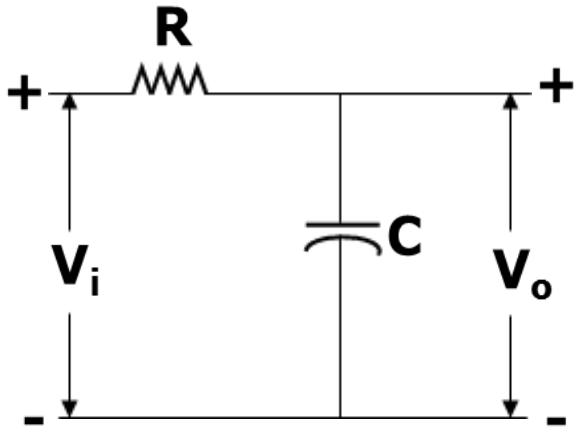
- The time constant of high pass RC circuit in very small in comparison within the time required for the input signal to make an appreciable change, the circuit is called a *"differentiator"*.
- Under this circumstances the voltage drop across R will be very small in comparison with the drop across C. Hence we may consider that the total input V_i appears across C, so that the current is determined entirely by the capacitance.
- Then the current is $i = C \frac{dV_i}{dt}$ and the output signal across R is

$$V_0 = iR$$

$$V_0 = RC \frac{dV_i}{dt}$$

- hence the output is proportional to the derivative of the input.

Low Pass RC Circuit



$$X_C = \frac{1}{2\Pi f C}$$

If f=low, X_c becomes high

C act as open circuit, so we get the output.

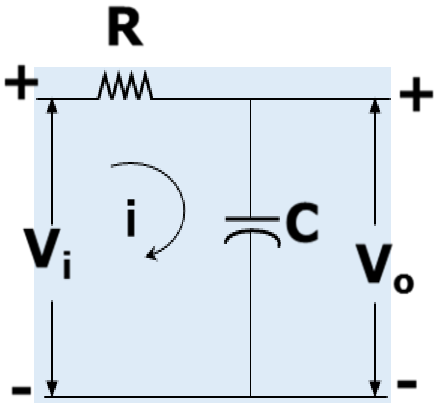
If f=high, X_c becomes low

C acts as short circuit, so V_o=0.

As the lower frequency signals appear at the output, it is called as "Low pass RC circuit".

Sinusoidal input

$$V_o = \frac{1}{CS} i$$



$$V_O = \frac{V_{in} \times \frac{X_C}{j}}{R + \frac{X_C}{j}}$$

where $X_C = \frac{1}{2\pi fC}$

$$V_O = \frac{V_{in} \times \frac{1}{j\,\omega C}}{R + \frac{1}{j\,\omega C}}$$

$$V_O = \frac{V_{in}}{j\omega RC + 1} = \frac{V_{in}}{1 + j2\pi fRC}$$

$$V_O = \frac{V_{in}}{1 + j\frac{f}{f_2}} \qquad \text{where } f_2 = \frac{1}{2\pi RC}$$

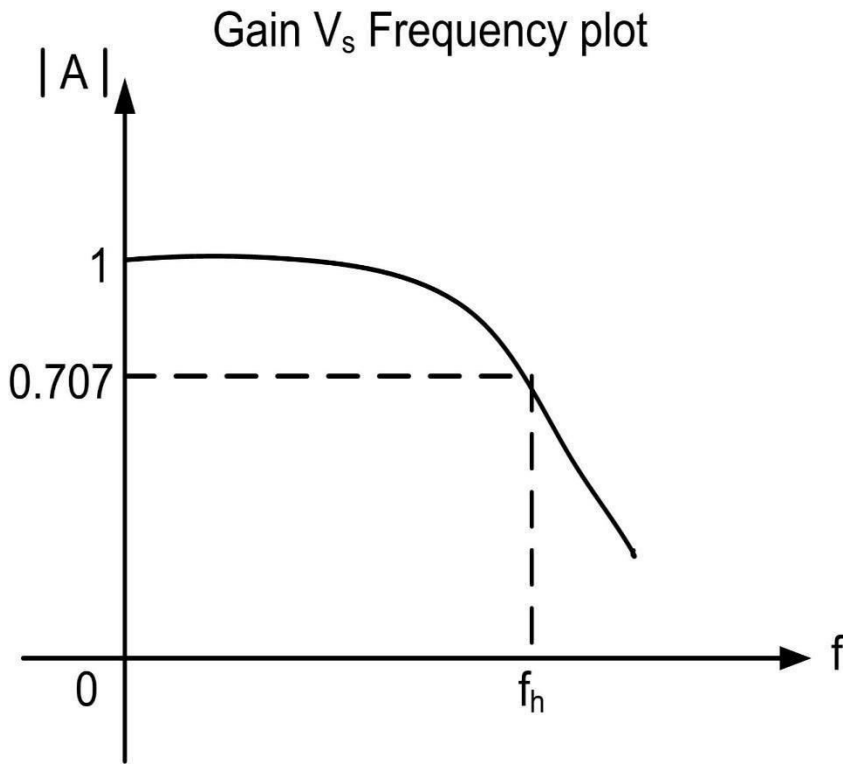
$$A = \frac{V_O}{V_{in}} = \frac{1}{1 + j\frac{f}{f_2}}$$

$$|A| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}} \qquad \text{and} \qquad \theta = -\tan^{-1}\left(\frac{f}{f_2}\right)$$

At the frequency $f = f_2$

$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707$$

$$|A| = 0.707$$



At $f = f_2$ the gain is 0.707 or this level corresponds to a signal reduction of 3 decibels(dB).

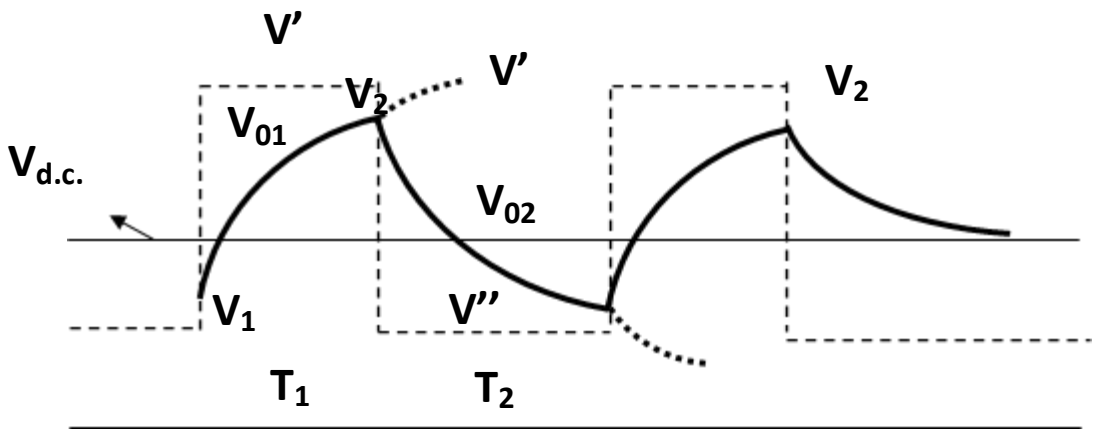
$\therefore$ f_2 or f_h is referred to as upper 3-dB frequency.

Square wave input

- Rise Time(t_r):

The time required for the voltage to rise from 10 $\%$ to 90$\%$ of the final steady value is called "Rise Time".

$$t_r = 2.2RC$$



$$\Rightarrow V_O = V_f + (V_i - V_f)\, e^{\frac{-t}{RC}}$$

The output voltage V_{01} & V_{02} is given by

$$V_{01} = V^1 + (V1 - V^1) \cdot e^{-T_1/RC} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V_{02} = V^{11} + (V2 - V^{11}) \cdot e^{-T_2/RC} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

if we set $V_{01} = V_2$ at $t = T_1$

and $V_{02} = V_1$ at $t = T_1 + T_2$

$$V_2 = V^1 + (V1 - V^1)\, e^{-T_1/RC}$$

$$V_1 = V^{11} + (V2 - V^{11})\, e^{-T_2/RC}$$

Since the average across R is zero then the d.c voltage at the output is same as that of the input. This average value is indicated as Vd.c.

Consider a symmetrical square wave with zero average value, so that

$$T_1 = T_2 = T/2$$

$$V^1 = -V^{11} = V/2 \quad \& \quad V_1 = -V_2$$

$$V_2 = \frac{V}{2} + \left(-V_2 - \frac{V}{2}\right) e^{-\frac{T}{2RC}}$$

$$V_2 = \left[1 + e^{-\frac{T}{2RC}}\right] = \frac{V}{2}\left[1 - e^{-\frac{T}{2RC}}\right]$$

$$V = \frac{V}{2}\left[\frac{1 - e^{-T/2RC}}{1+e^{-T/2RC}}\right]$$

$$V_2 = \frac{V}{2}\left[\frac{e^{T/2RC} - 1}{e^{T/2RC} + 1}\right]$$

$$V_2 = \frac{V}{2} \cdot \frac{e^{2x} - 1}{e^{2x} + 1} \text{ where } x = \frac{T}{4RC}$$

$$V_2 = \frac{V}{2} \tan hx$$

Low pass RC circuit acts as an integrator

- The time constant is very large in comparison with the time required for the input signal to make an appreciable change, the circuit is called an "Integrator".
- As RC>>T the voltage drop across C will be very small in comparison to the voltage drop across R and we may consider that the total input V_i appear and across R, then

$$V_i = iR$$

$$i = \frac{V_i}{R}$$

For low pass RC circuit the output voltage V_o is given by

$$V_o = \frac{1}{C}\int i\,dt$$

$$V_o = \frac{1}{C}\int \frac{V_i}{R}\,dt$$

$$V_o = \frac{1}{RC}\int V_i\,dt$$

Advantages of Integrator over differentiator

- Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons.

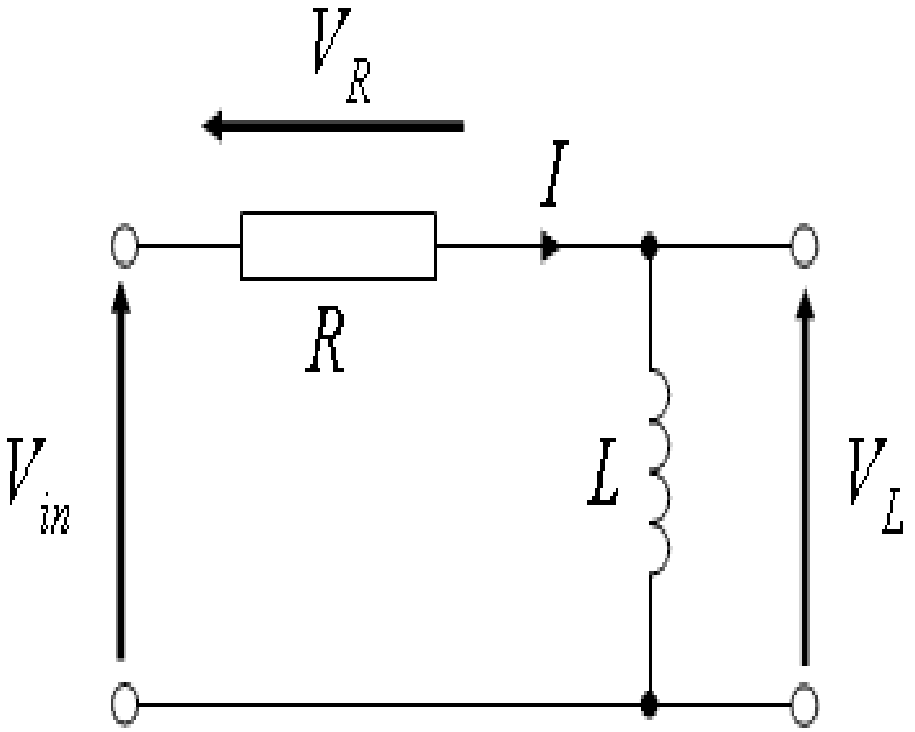
- The gain of the integrator decreases with frequency where as the gain of the differentiator increases linearly with frequency. It is easier to stabilize the former than the latter with respect to spurious oscillations.

- As a result of its limited band width an integrator is less sensitive to noise voltages than a differentiator.

- If the input wave form changes very rapidly, the amplifier of a differentiator may over load.

- It is more convenient to introduce initial conditions in an integrator.

RL Circuits



- **RL filter** or **RL network**, is an electric circuit composed of resistors and inductors driven by a voltage or current source
- $X_L = \omega L$

UNIT-2

NON-LINEAR WAVE SHAPING

Non-Linear Wave Shaping

Definition: The process where by the form of a signal is changed by transmission through a non-linear network is called Non-linear Wave Shaping.

Types:

i. Clippers.

ii. Clampers.

Clipper Classifications

According to biasing, the clippers may be classified as

- Unbiased clippers and
- Biased clippers.

According to configuration used the clippers may be

- Series diode clippers
- Parallel or shunt diode clippers
- A series combination of diode, resistor and reference supply
- Multi-diode clippers consisting of several diodes, resistors and reference voltages
- Two emitter-coupled transistors operating as an over-driven

Contd…

According to level of clipping the clippers may be

- Positive clippers
- Negative clippers
- Biased clippers and
- Combination clippers

Clipper

- Clipping circuits are used to remove the part of a signal that is above or below some defined reference level.

•Clippers also known as

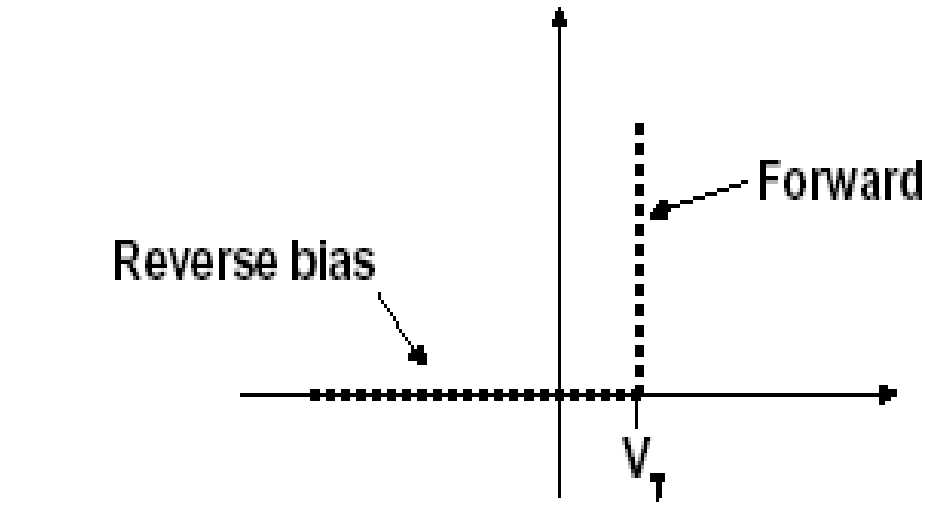
Voltage limiters

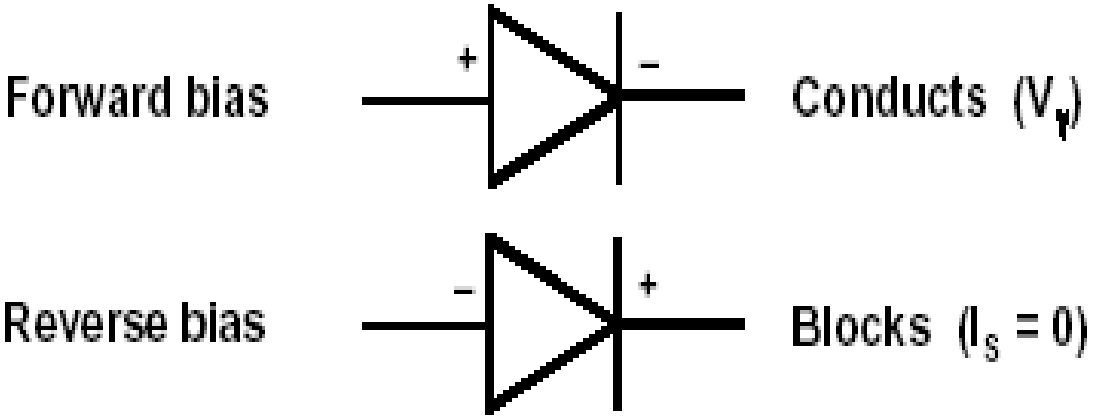
Current limiters

Amplitude selectors

Slicers

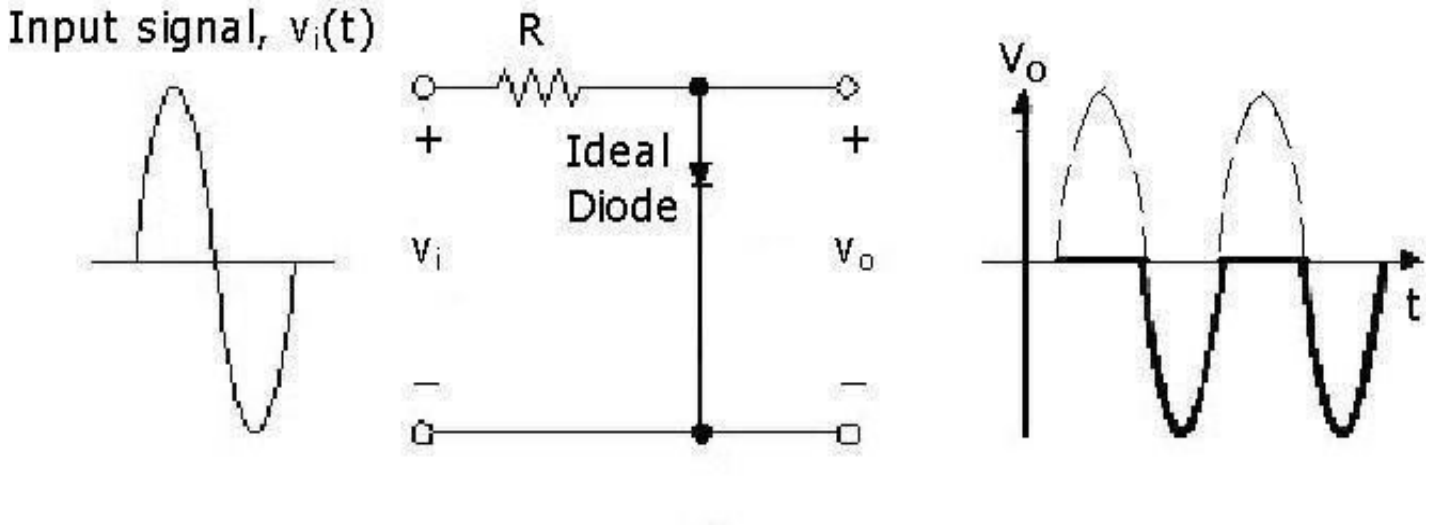
Let's again consider piecewise linear diode model





Unbiased clippers(Parallel PositiveClippers)

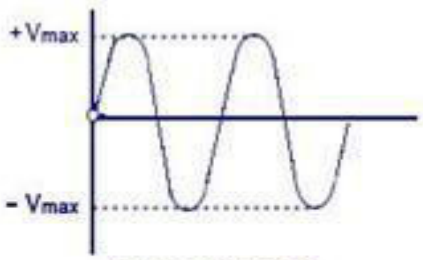
- **Without** the battery, the output of the circuit below would be the negative portion of the input wave (assuming the bottom node is grounded). When *vi* > 0, the diode is on (short-circuited), *vi* is dropped across R and *vo*=0. When *vi* <0, the diode is off (open-circuited), the voltage across R is zero and *vo*=*vi*.

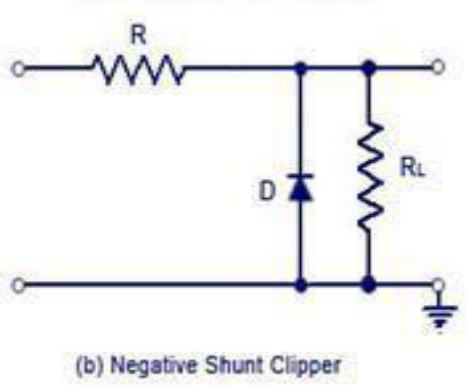


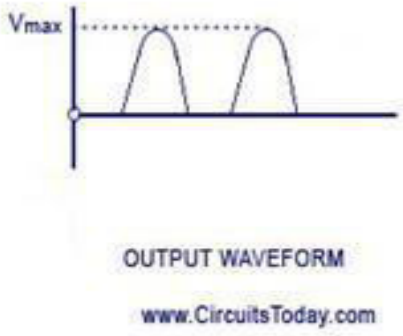
Unbiased clippers(Parallel Negative Clippers)

+ive cycle :- anode is at ground potential and cathode sees variable +ive voltage from 0 to +Vm So complete cycle, the diode is reverse biased and Vo =Vin.At positive peak Vo=+5V

-ive cycle :- anode is at ground potential and cathode sees variable -ive vols from 0 to –Vm. When magnitude of in put volatge i.e / Vin/ >Vd, the diode become forward biased and hence Vo =-Vd =0.7V



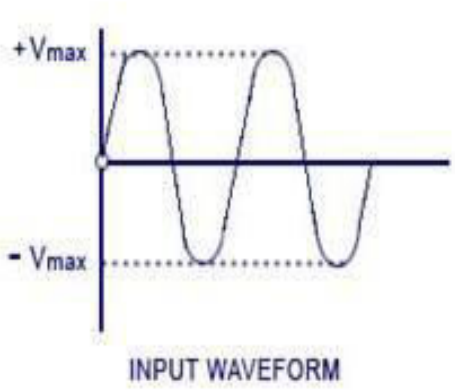




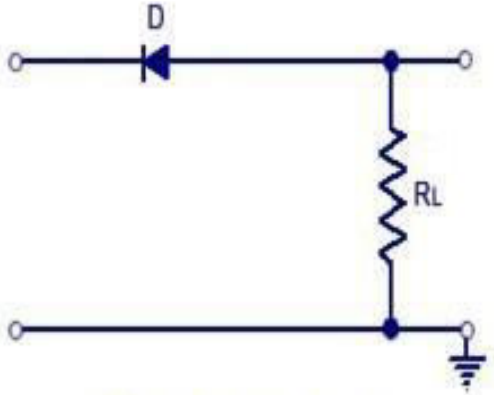
Series positive clipper

+ive cycle :- anode is at ground potential and cathode sees variable +ive voltage from 0 to +Vm. For comlpete, cycle, diode become reverse biased and hence Vo=0V

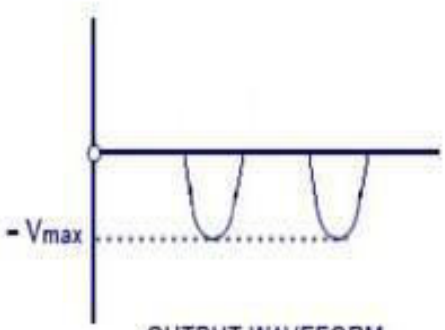
-ive cycle :- anode is at ground potential and cathode sees variable -ive voltage from 0 to –Vm. So in complete cycle, the diode is forward biased and Vo= Vin + Vd andAt negative peak,



INPUT WAVEFORM



(a) Positive Series Clipper

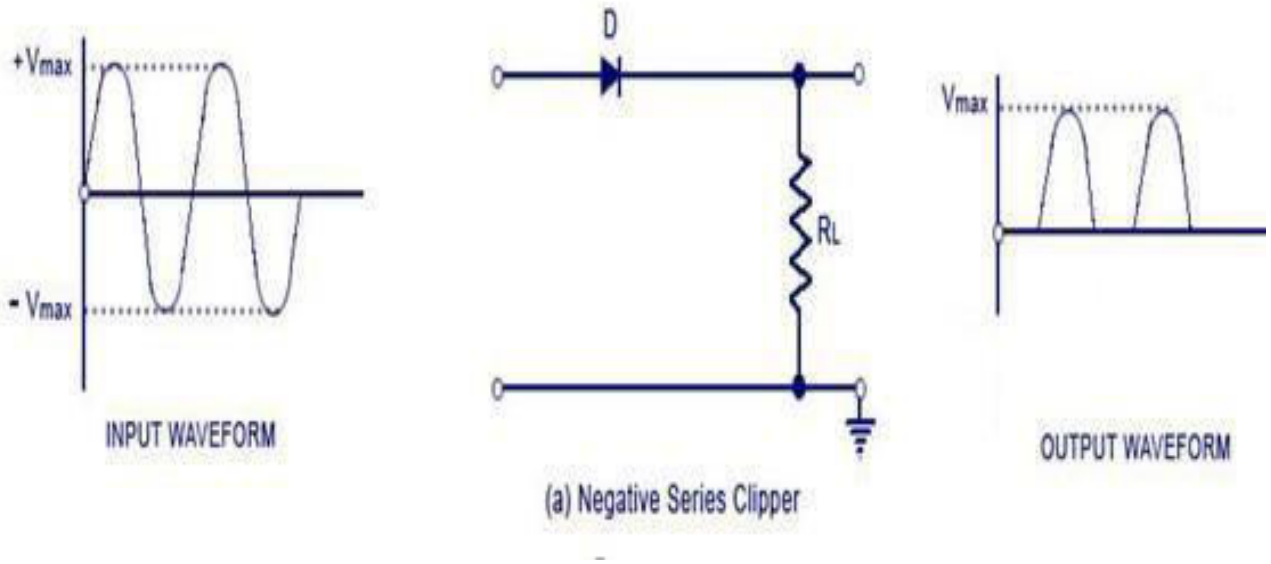


OUTPUT WAVEFORM

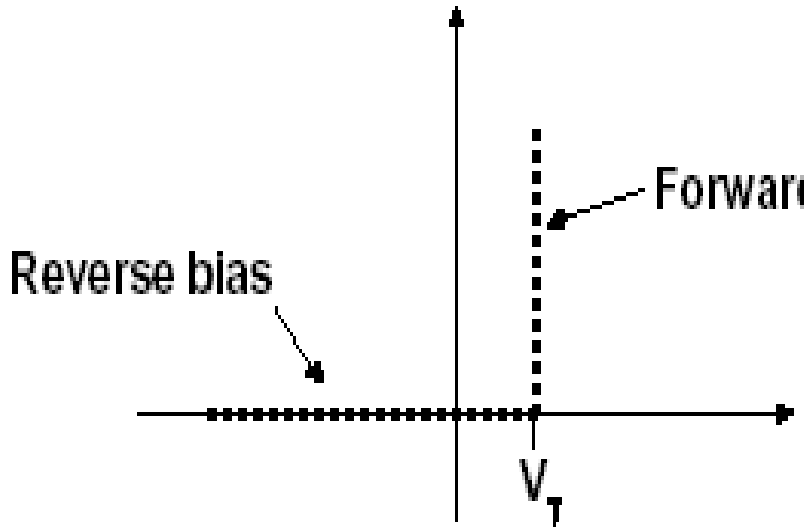
Series Negative clipper

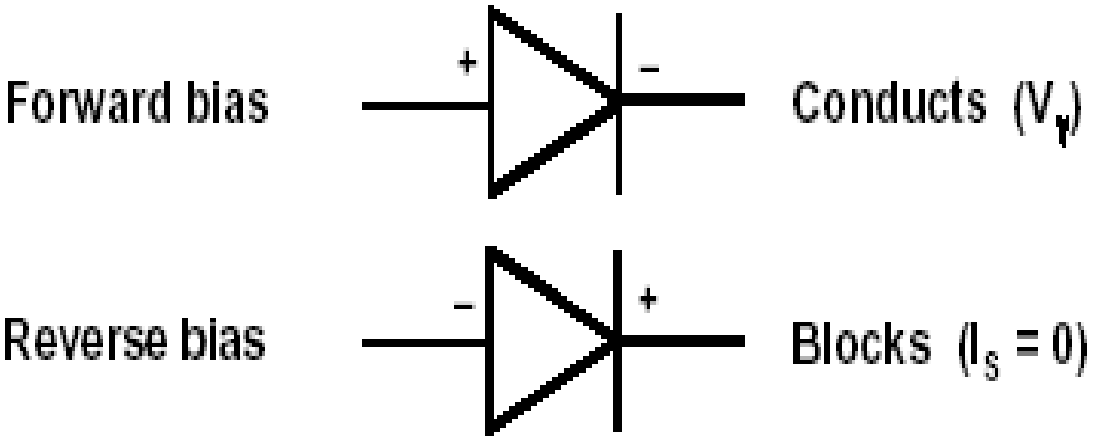
+ive cycle :- anode is at positive potential from 0 to +Vm.For comlpete, cycle, diode become forward biased and hence vo= 5v

-ive cycle :- Cathode is at ground potential and cathode sees variable -ive voltage from 0 to –Vm. So in complete cycle, the diode is Reverse biased and negative peak, Vo= 0

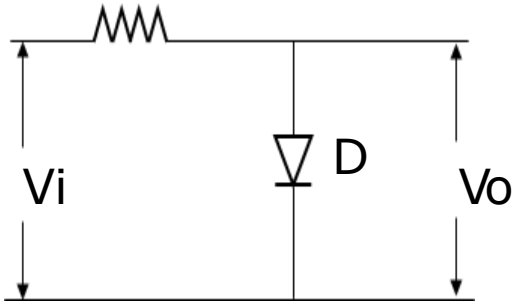


Let's again consider piecewise linear diode model





Positive Shunt clipping with zero reference voltage



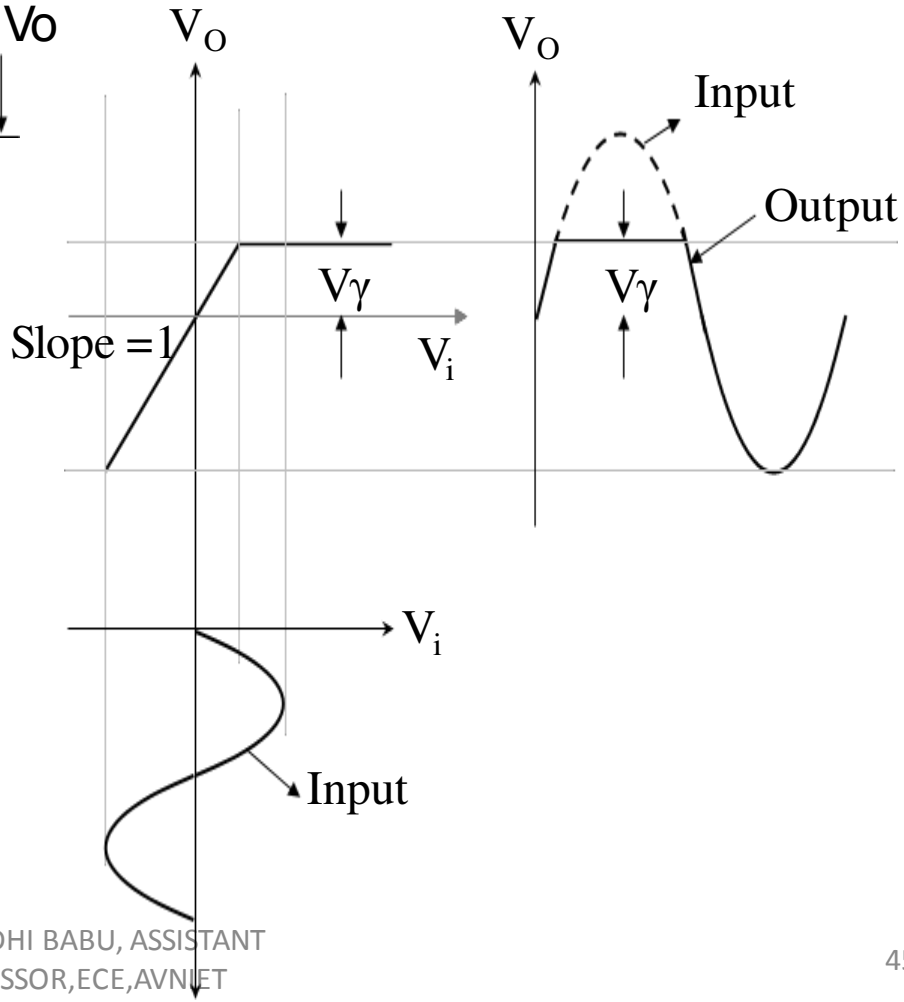
Transfer characteristics equations:

$V_O = 0$ for $V_i > 0$

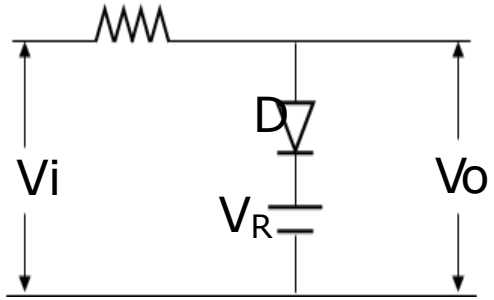
$V_O = V_i$ for $V_i < 0$ } [Ideal]

$V_O = V_\gamma$ for $V_i > V_\gamma$ D – ON

$V_O = V_i$ for $V_i < V_\gamma$ D – OFF



Positive Shunt clipping with positive reference voltage V_R



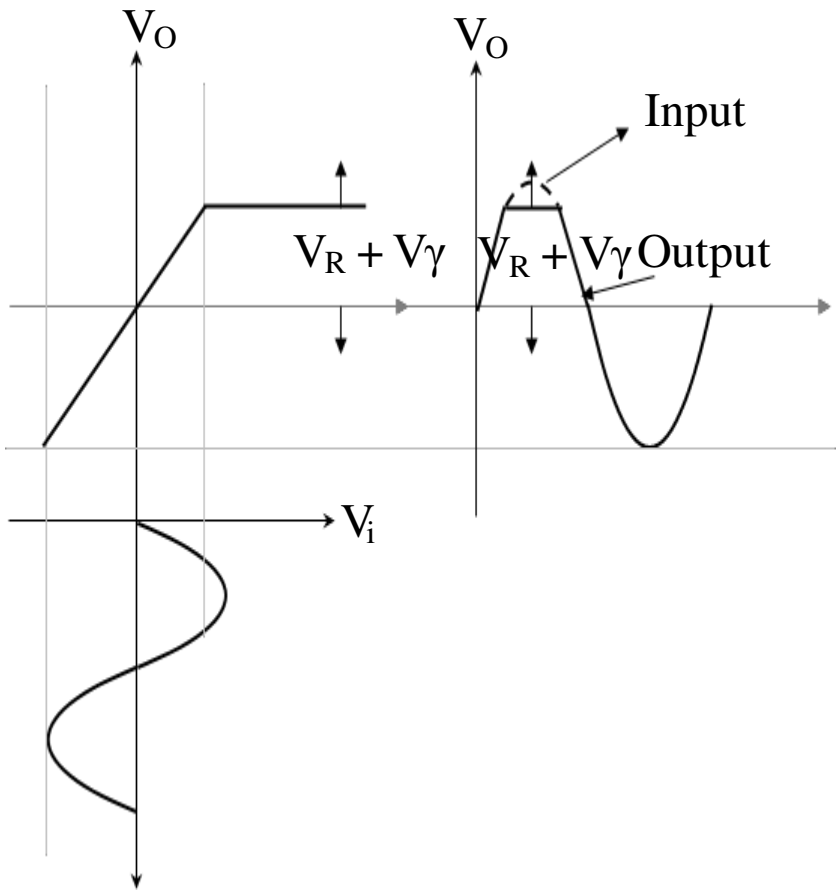
Transfer characteristics equations:

$V_i < V_R+V\gamma$ D – OFF

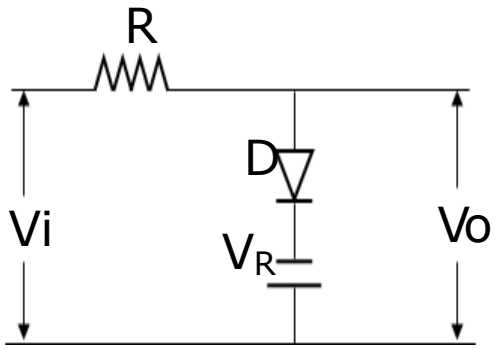
$V_O = V_i$

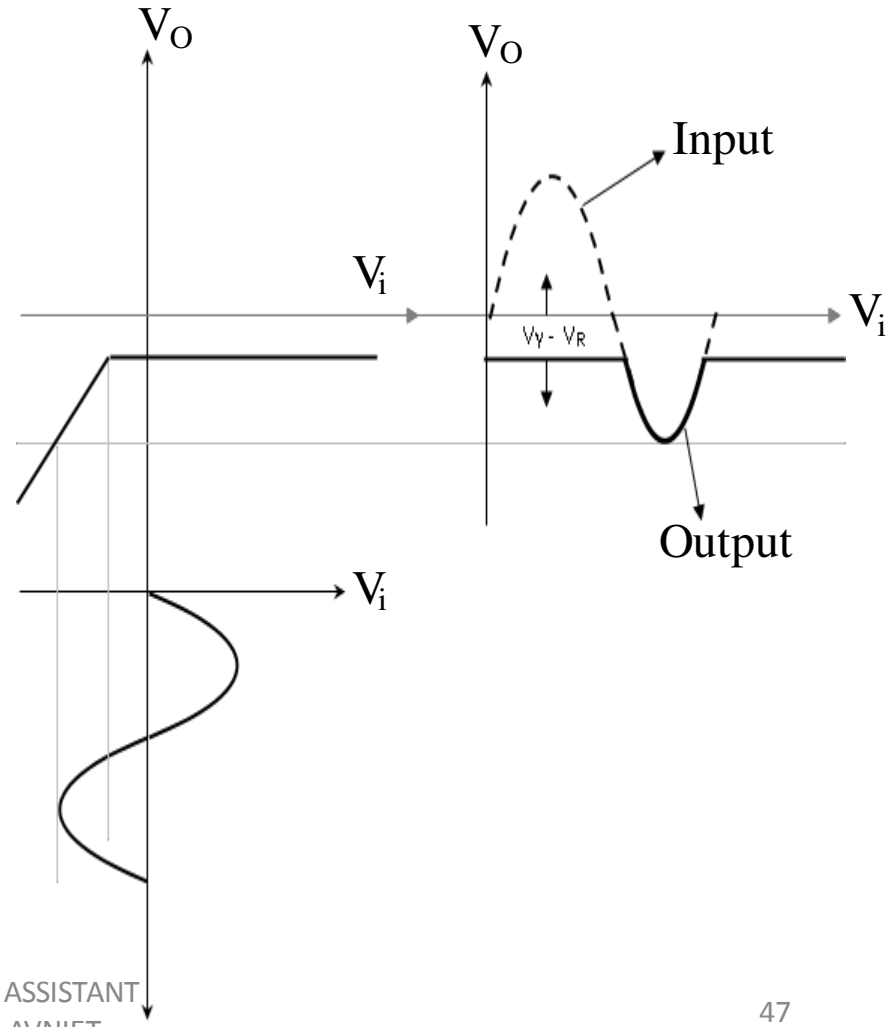
$V_i > V_R+V\gamma$ D – ON

$V_O = V_R+V\gamma$



Positive Shunt clipping with negative reference voltage





Transfer characteristics equation:

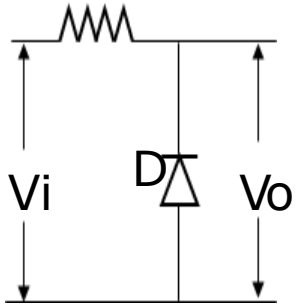
$V_i > V\gamma - V_R$ D – ON V_O

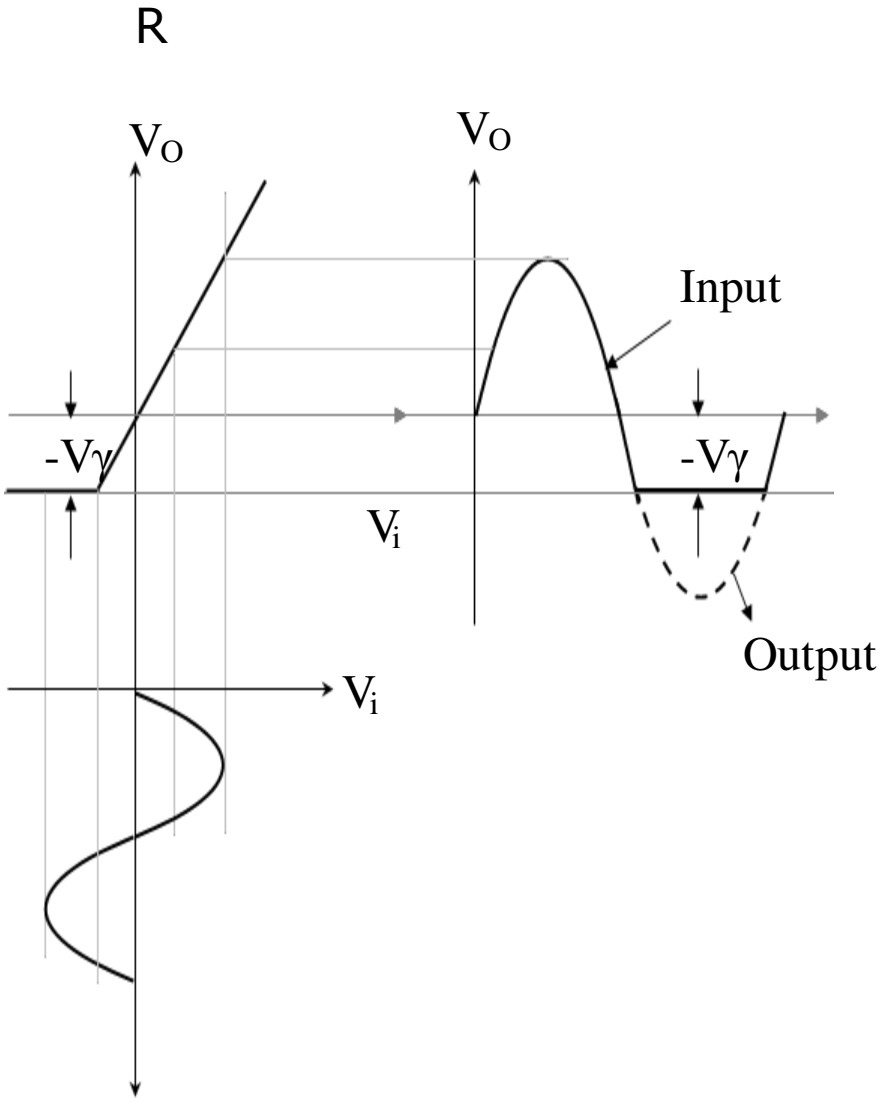
$= V\gamma - V_R$

$V_i < V\gamma - V_R$ D – OFF

$V_O = V_i$

Negative Shunt clipping with zero reference voltage



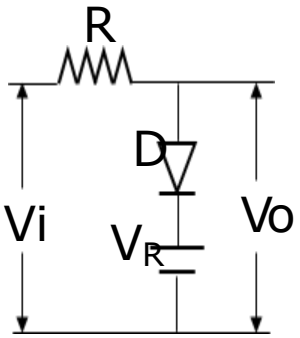


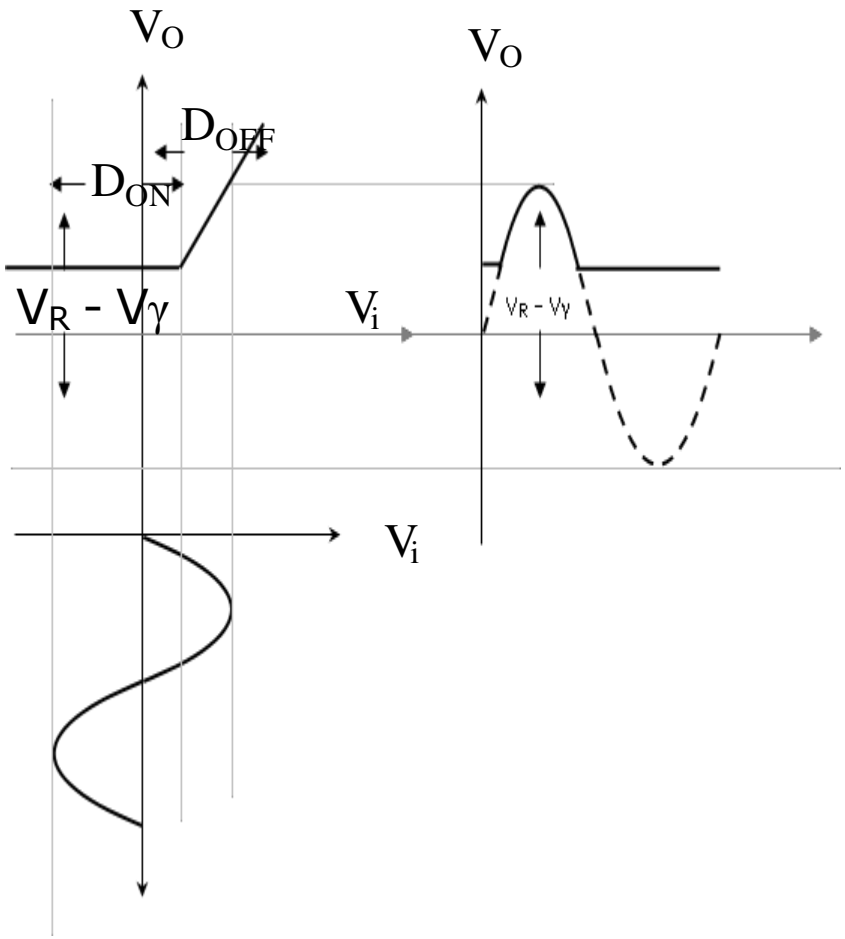
Transfer characteristic equations:

$V_i > -V\gamma$ D – OFF $V_O = V\gamma$

$V_i < -V\gamma$ D – ON $V_O = -V\gamma$

Negative Shunt clipping with positive reference voltage





Transfer characteristics equations:

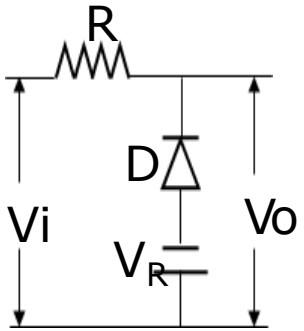
$V_i < V_R - V_\gamma$ D – ON

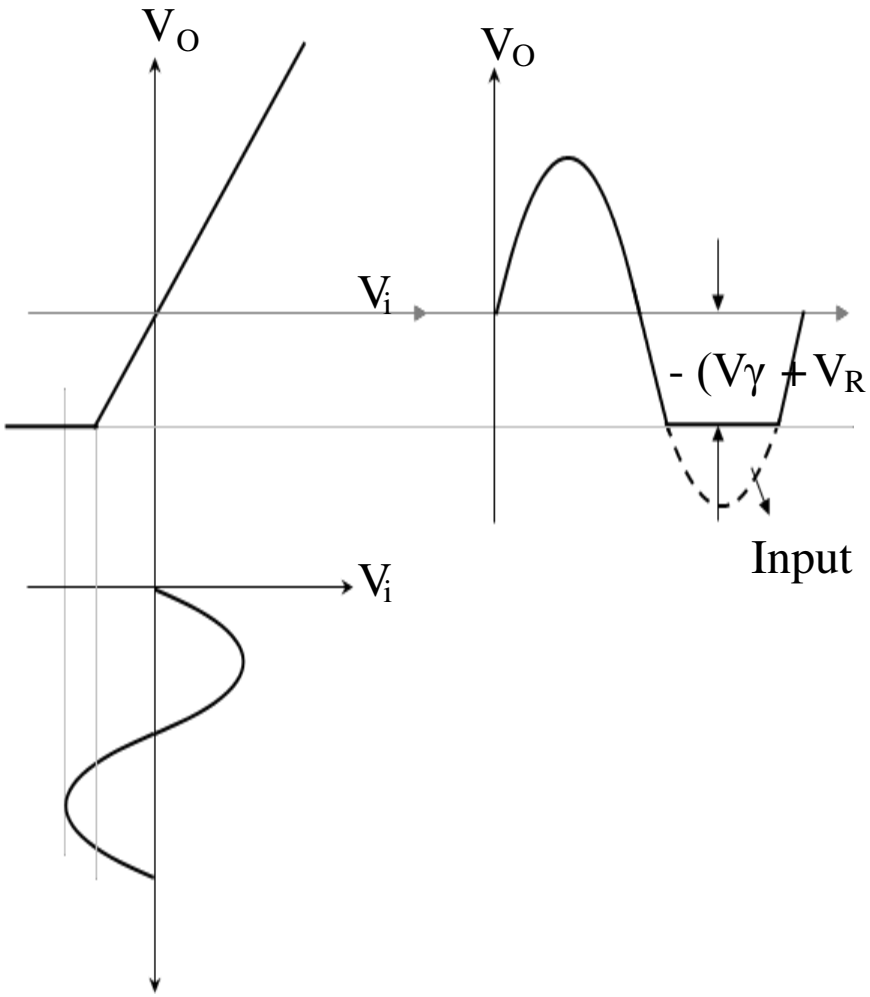
$V_O = V_R - V_\gamma$

$V_i > V_R - V_\gamma$ D – OFF

$V_O = V_i$

Negative Shunt clipping with negative reference voltage



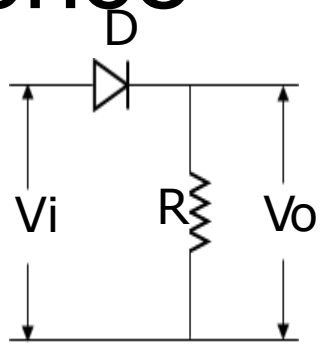


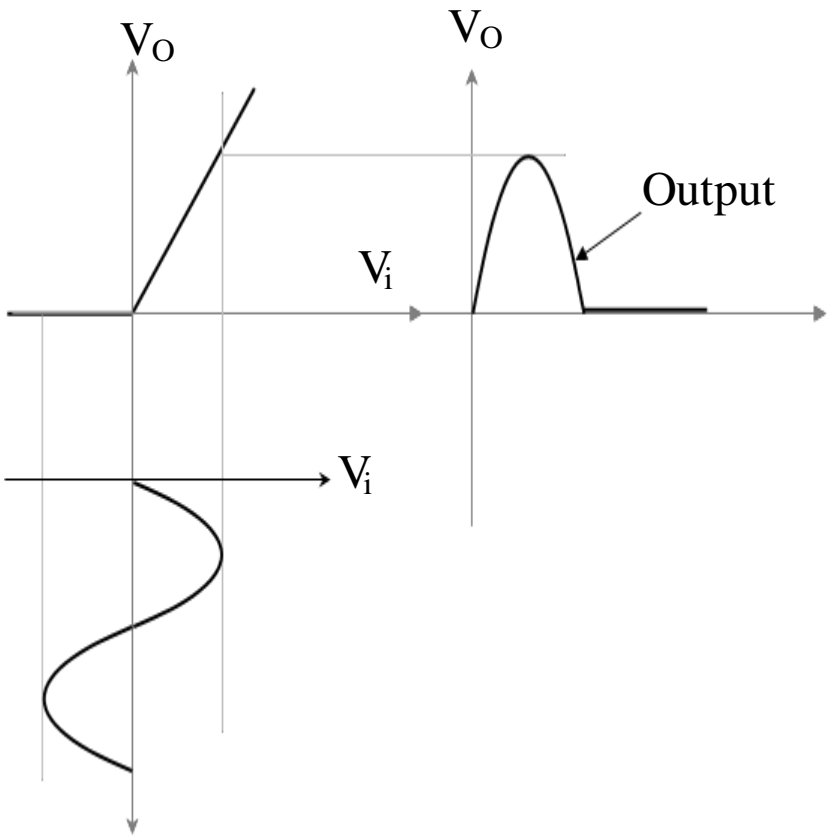
Transfer characteristic equations:

$V_i < -(V\gamma + V_R)$ D – ON $V_O = -(V\gamma + V_R)$

$V_i < -(V\gamma + V_R)$ D – OFF $V_O = V_i$

Negative Series clipper with zero reference

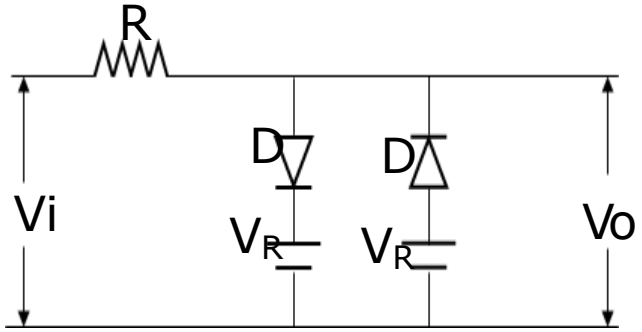




Transfer characteristic equations:

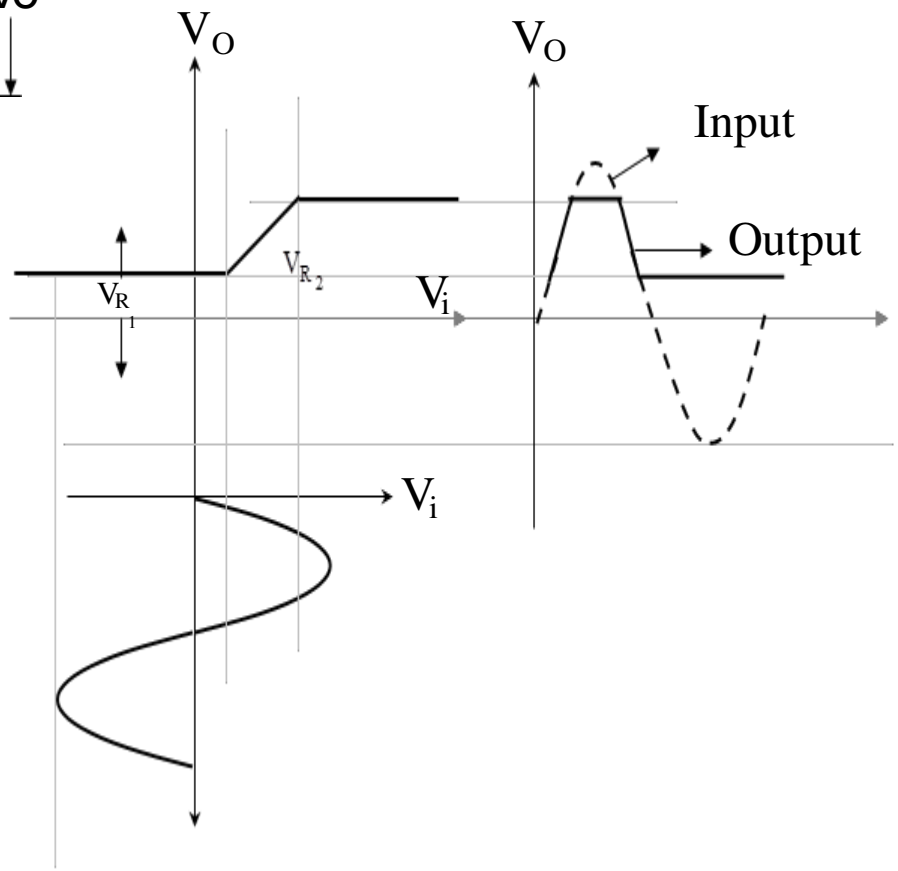
$V_i<0$	D–OFF	$V_O=0$	Ideal Diode
$V_i>0$	D-ON	$V_O=V_i$	
$V_i<V_\gamma$	D–OFF	$V_O=0$	Practical Diode
$V_i>V_\gamma$	D-ON	$V_O=V_i-V_\gamma$	

CLIPPING ATTWO INDEPENDENT LEVELS

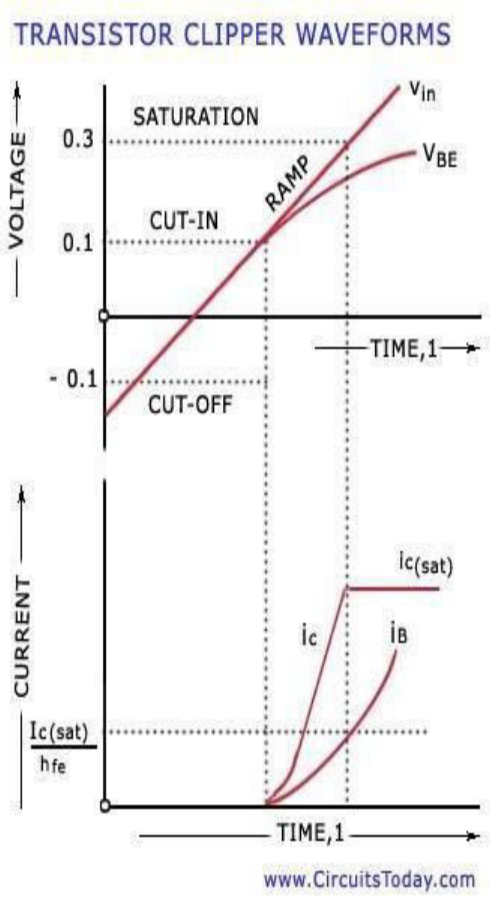


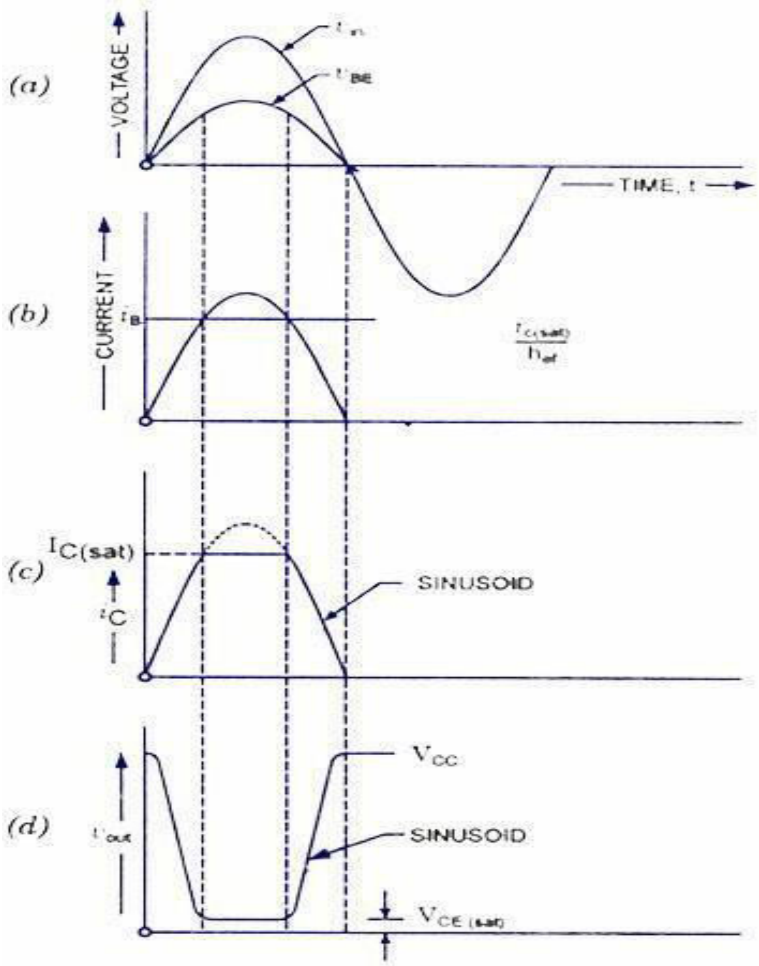
Transfercharacteristic equations;

Input (V_i)	DiodeState	Output (V_o)
$V_i \le V_{R_1}$	D_1 –ON, D_2 – OFF	$V_O = V_{R_1}$
$V_{R_1} < V_i < V_{R_2}$	D_1 –OFF, D_2 – OFF	$V_O = V_i$
$V_i \ge V_{R_2}$	D_1 –OFF, D_2 – ON	$V_O = V_{R_2}$



Contd..



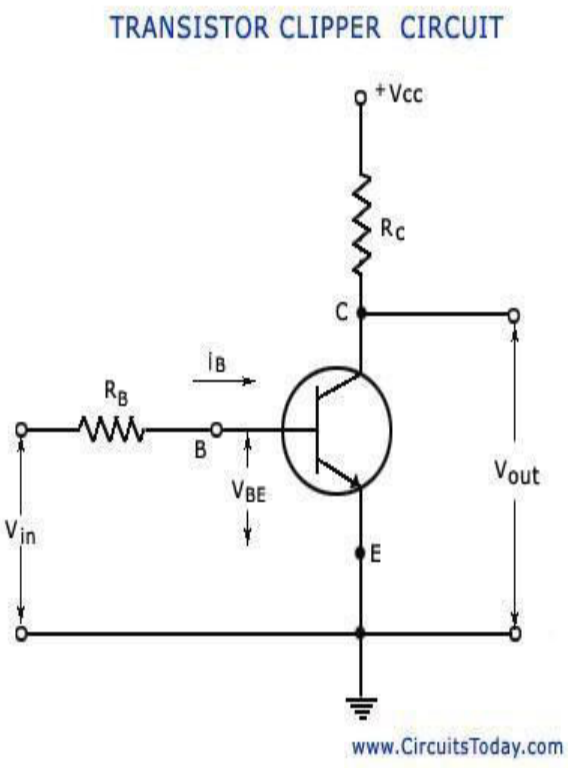


Transistor Clipper Waveforms For Sinusoidal Input

Transistor Clipper circuit

- The transistor has two types of linearities

—One linearity happens when the transistor passes from cut-in region to the active region. The other linearity occurs when the transistor passes from the active region to the saturation region. When any input signal passes through the transistor, across the boundary between cut-in region and active region, or across the boundary between the active region and saturation region, a portion of the input signal ff



CLAMPING CIRCUIT

- The need to establish the extremity of the positive (or) negative signal excursion at some reference level. When the signal is passed through a capacitive coupling network such a signal has lost its d.c. component. The clamping circuit introduces the d.c. components at the outside, for this reason the coupling circuits are referred to as d.c. restore (or) d.c. reinserter.

- Def : " A clamping circuit is one that takes an input waveform and provides an output i.e., a faithful replica of its shape, but has one edge clamped to the zero voltage reference point.

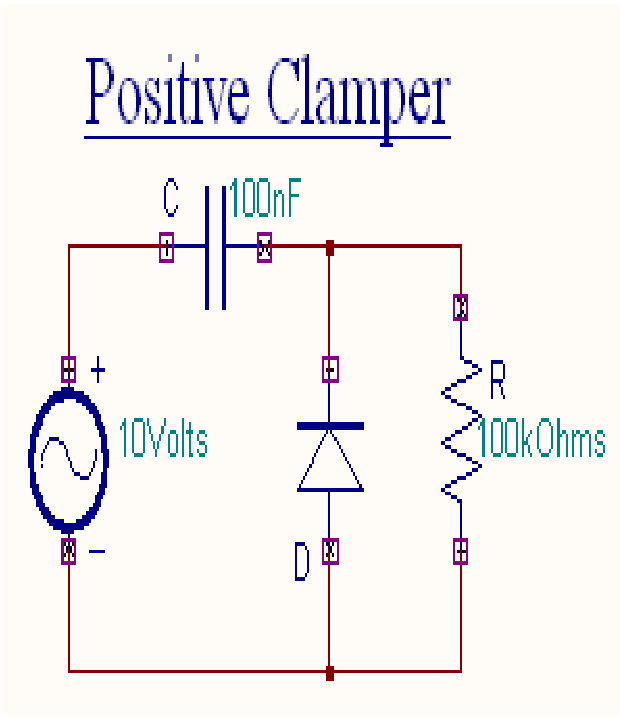
There are two types of clamping circuits.

- 1) Negative clamping circuit.
- 2) Positive clamping circuit.

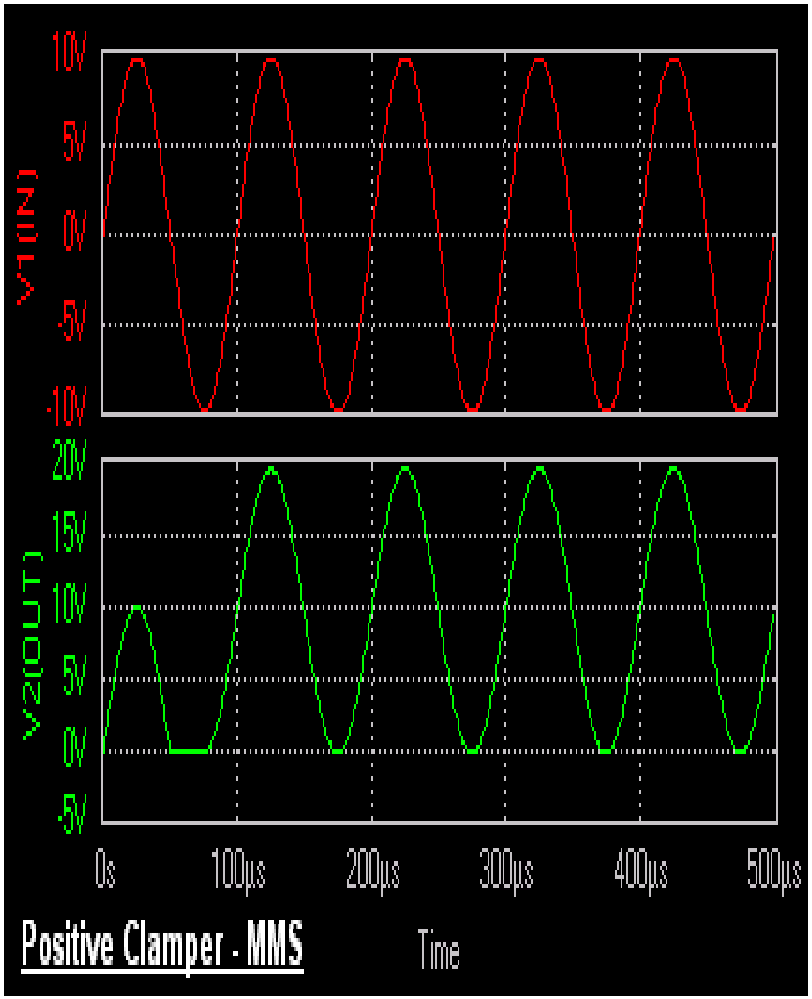
Diode :- Clamper

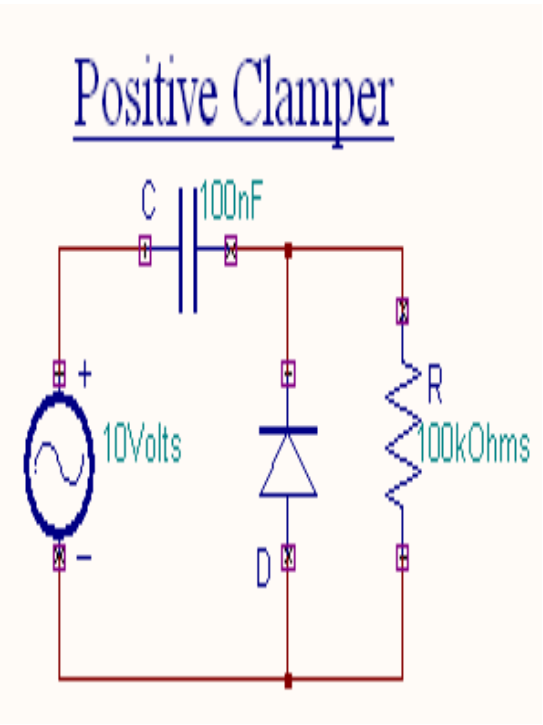
Positive Clamper

The circuit for a positive clamper is shown in the figure. During the negative half cycle of the input signal, the diode conducts and acts like a short circuit. The output voltage $V_o \Rightarrow 0$ volts . The capacitor is charged to the peak value of input voltage V_m. and it behaves like a battery. During the positive half of the input signal, the diode does not conduct and acts as an open circuit. Hence the output voltage $V_o \Rightarrow V_m + V_m$ This gives a positively clamped voltage.



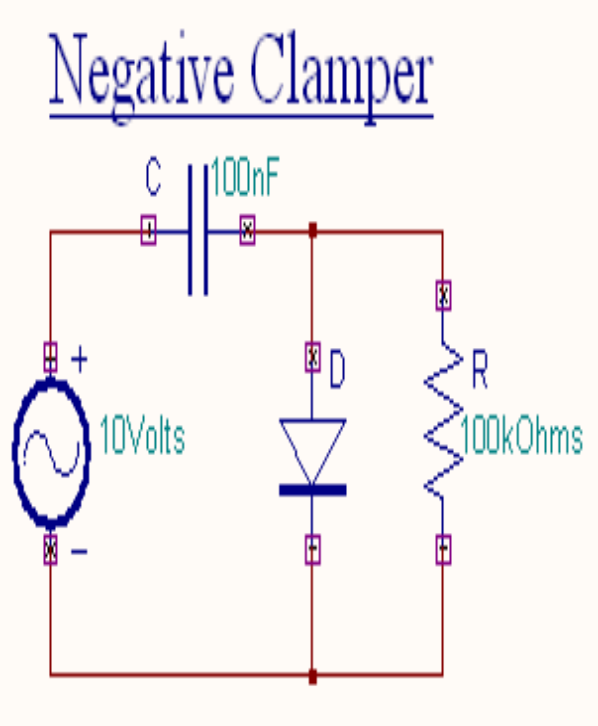
$V_o \Rightarrow V_m + V_m = 2V_m$


10V
5V
0V
-5V
-10V
V1(IN)
20V
15V
10V
5V
0V
-5V
V2(OUT)
0s
100µs
200µs
300µs
400µs
500µs
Positive Clamper - MMS
Time

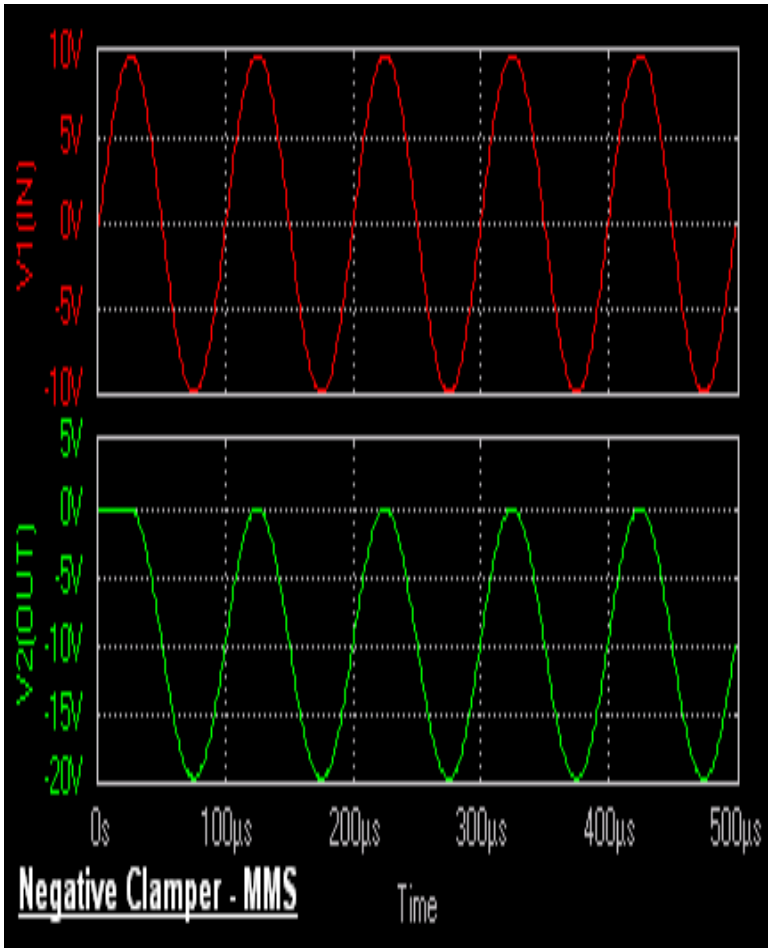

Positive Clamper
C
100nF
+
10Volts
−
D
R
100kOhms

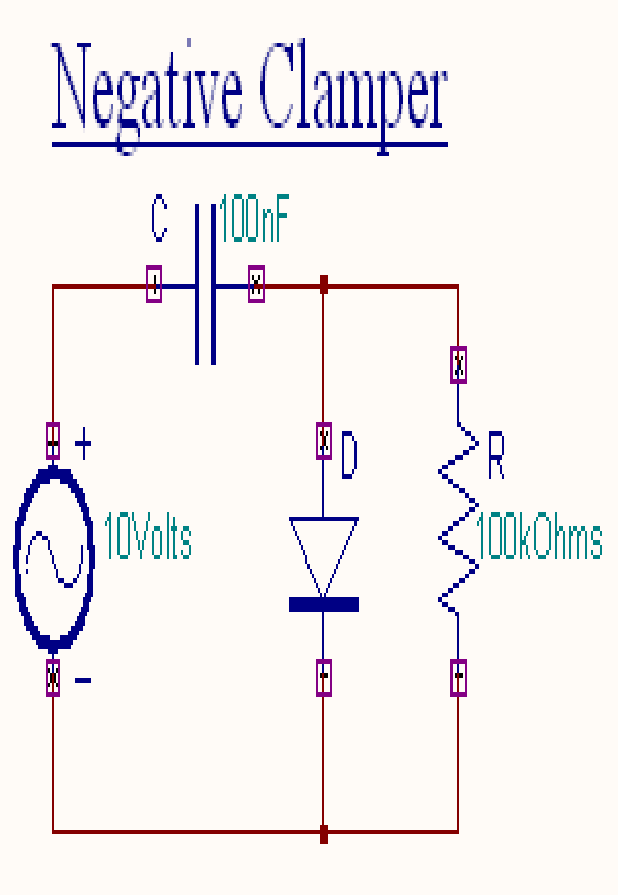
Negative Clamper

During the positive half cycle the diode conducts and acts like a short circuit. The capacitor charges to peak value of input voltage V_m. During this interval the output *Vo* which is taken across the short circuit will be zero During the negative half cycle, the diode is open. The output voltage can be found by applying KVL.

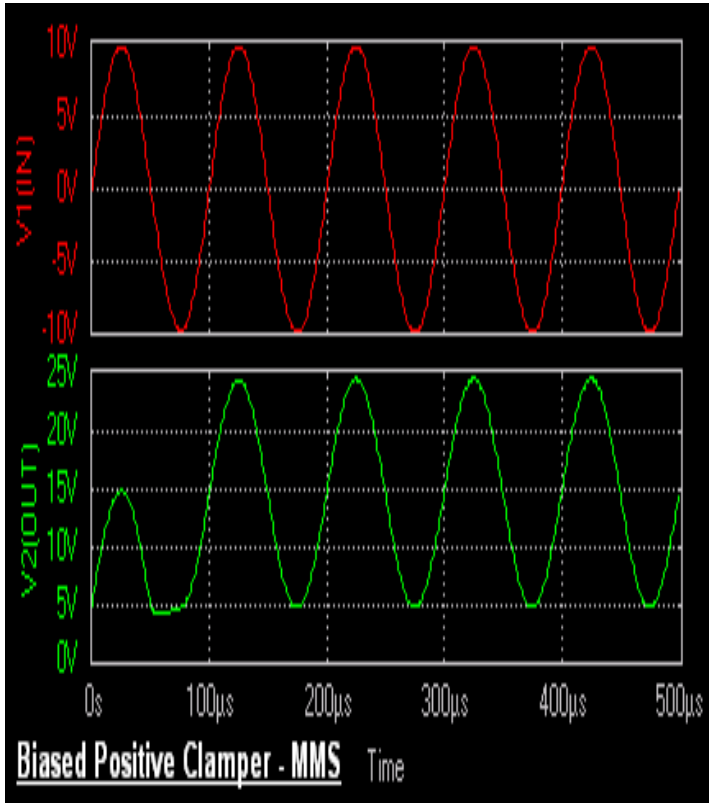


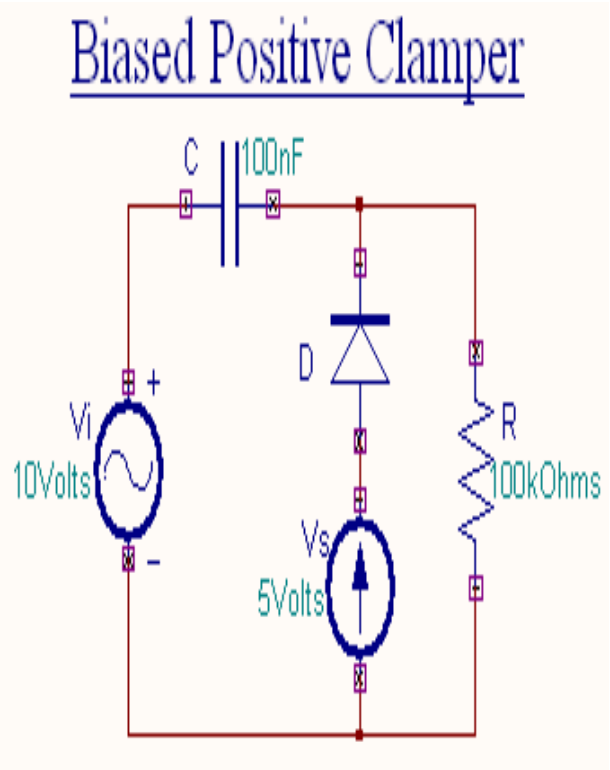
$$-V_m - V_m - V_o = 0 \qquad V_o = -2V_m$$


10V
5V
0V
-5V
-10V
V1(IN)
5V
0V
-5V
-10V
-15V
-20V
V2(OUT)
0s
100µs
200µs
300µs
400µs
500µs
Time
Negative Clamper - MMS


Negative Clamper
C
100nF
+
10Volts
-
D
R
100kOhms

Biased Clamper





CLAMPING CIRCUIT THEOREM

- Therefore the charge acquired by the capacitor during the forward interval

$$\therefore \frac{A_f}{A_r} = \frac{R_f}{R}$$

Consider a square wave input is applied to a clamping circuit under steady state condition

If $V_f(t)$ is the output waveform in the forward direction, then from below figure the capacitor charging current is

$$i_f = \frac{V_f}{R_f}$$

Therefore the charge acquired by the capacitor during the forward interval

$$\int_0^{T_1} i_f dt = \frac{1}{R_f}\int_0^{T_1} V_f\, dt = \frac{A_f}{R_f} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

•Similarly if $V_f(t)$ is the output voltage in the reverse direction, then the current which discharges by the capacitor is

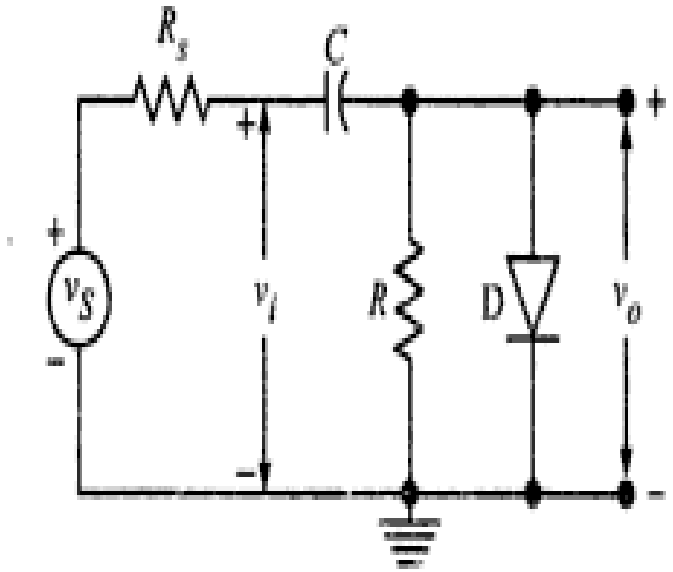
$$i_r = \frac{V_r}{R}$$

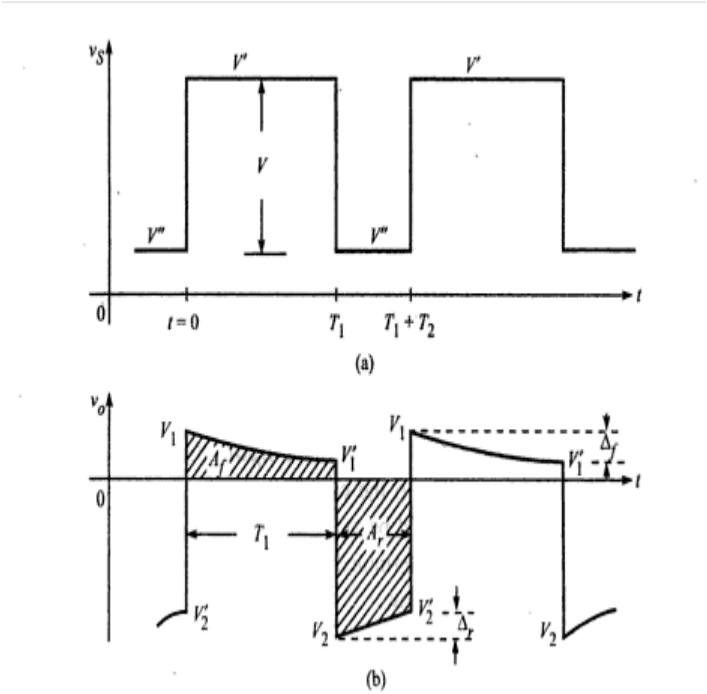
$$\int_{T_1}^{T_2} i_r \, dt = \frac{1}{R}\int_{T_2}^{T_2} V_r \, dt = \frac{A_r}{R} \quad \text{.....(2)}$$

In the steady-state the net charge acquired by the capacitor must be zero.

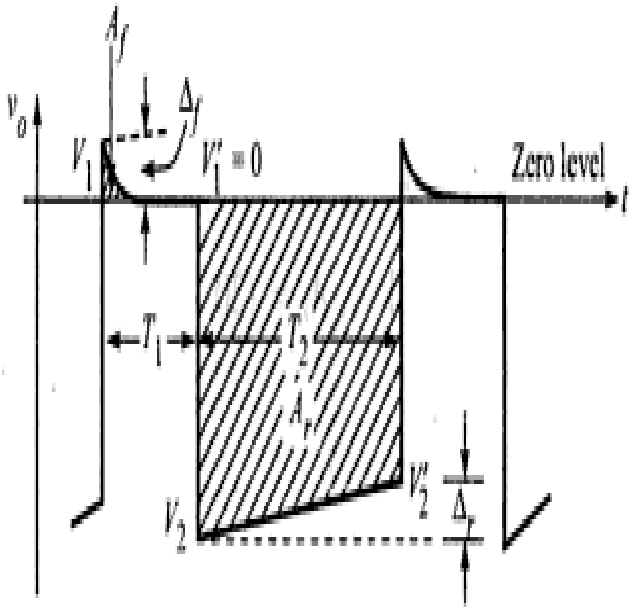
Therefore from equation (1) & (2) $\frac{A_f}{R_f} \frac{A_r}{R}$ this equation says that for any input waveform the ratio of the area under the output voltage curve in the forward direction to the reverse direction is equal to the ratio $\frac{R_f}{R}$.

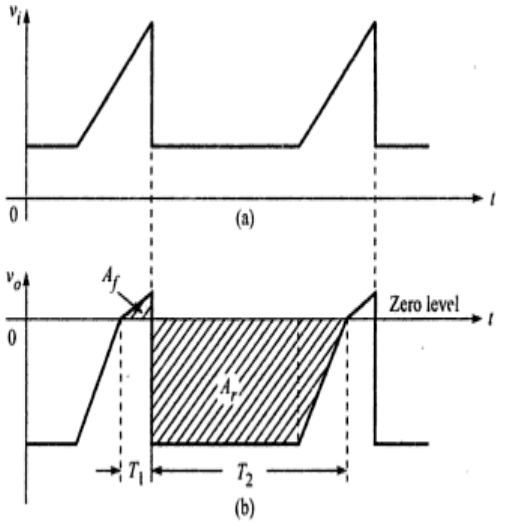
Clamping Circuit taking Source and Diode Resistances into account



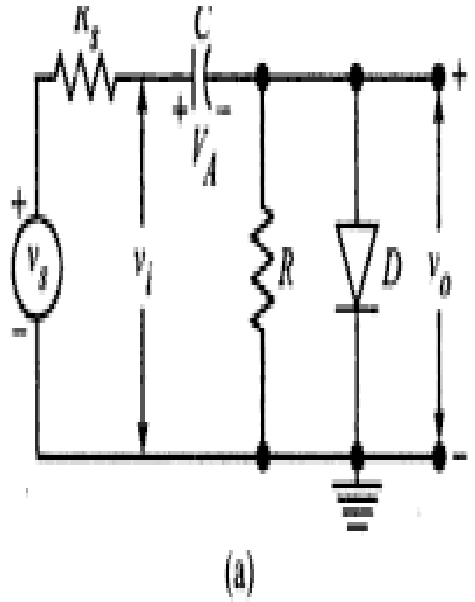


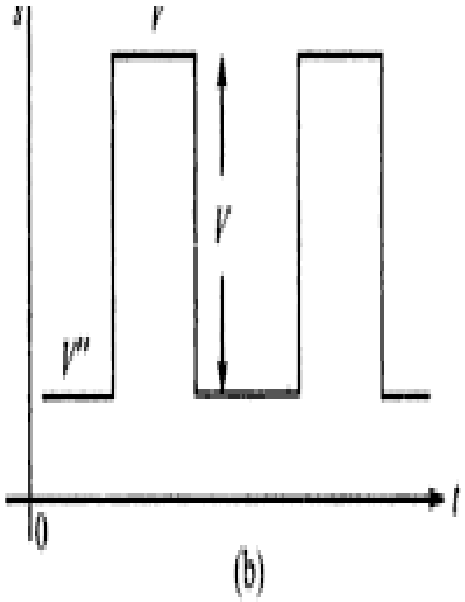
Practical Clamping circuit





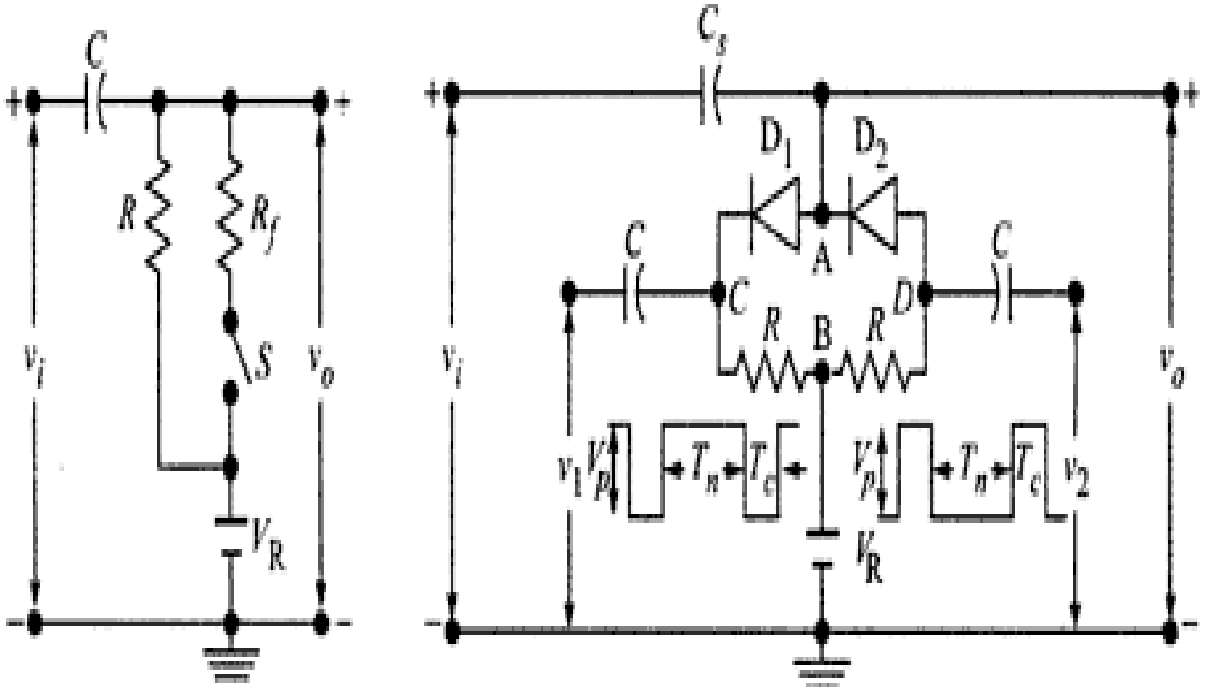
Effect of diode characteristics on clamping voltage





$$dV_{cl} = \eta V_T \frac{dV}{V}$$

Synchronized Clamping



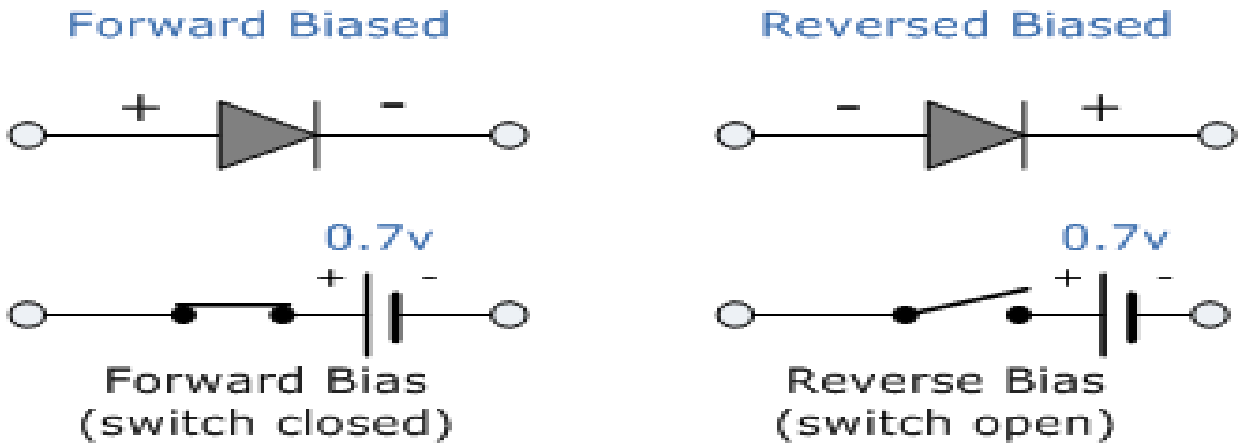
UNIT - 3

Steady State Switching Characteristics of Devices

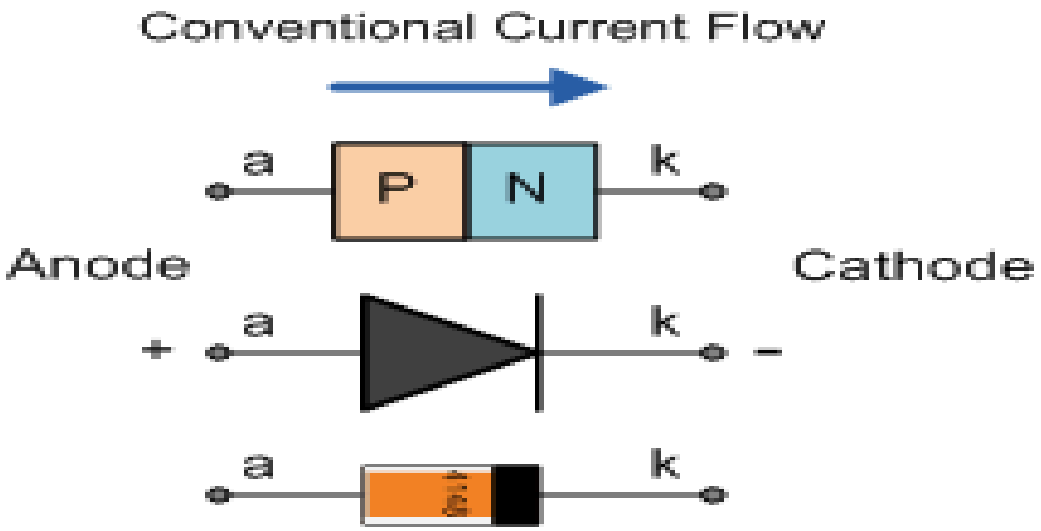
- **Transistors as switches**
  - both FETs and bipolar transistors make good switches
  - neither form produce *ideal* switches and their characteristics are slightly different
  - both forms of device take a finite time to switch and this produces a slight delay in the operation of the gate
  - this is termed the **propagation delay** of the circuit

Diode As a Switch

- The semiconductor Signal Diode is a small non-linear semiconductor devices generally used in electronic circuits, where small currents or high frequencies are involved such as in radio, television and digital logic circuits



Diode As a Switch



Silicon Diode and its
V-I Characteristics

Piece-wise linear model

- Unlike the resistor, whose two terminal leads are equivalent, the behavior of the diode depend on the relative polarity of its terminals.
- Ideal Diode

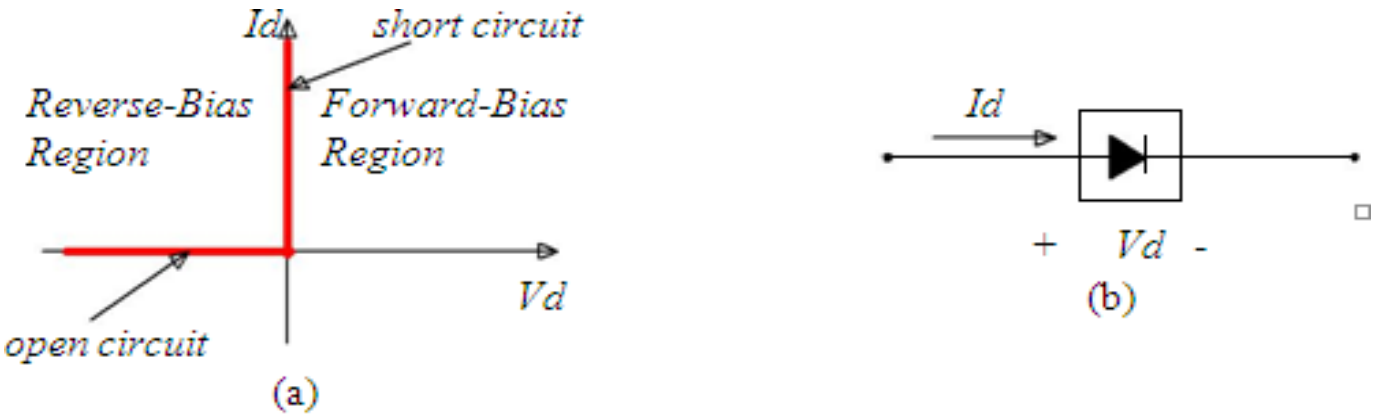
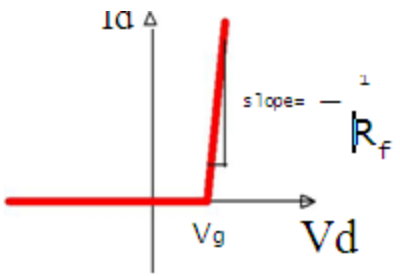
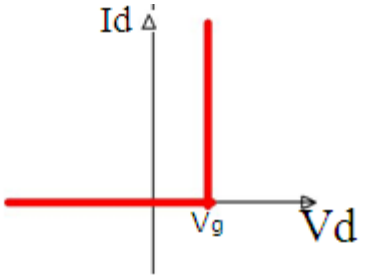


Figure 2. I-V characteristic (a) and symbol (b) of the ideal diode.

Contd….

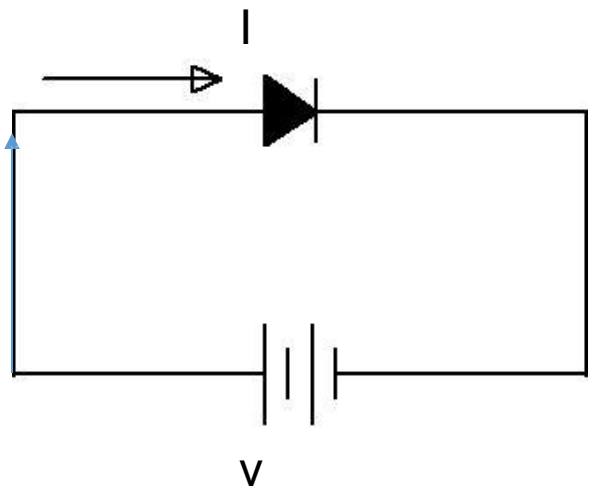


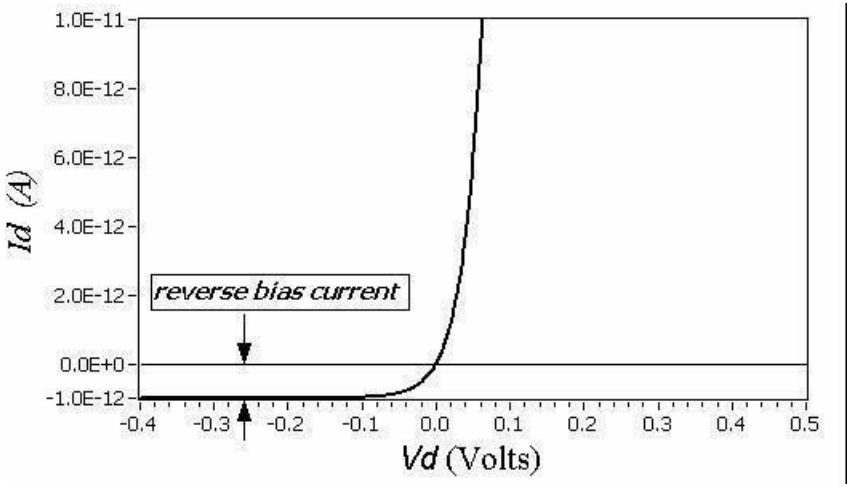
Piecewise linear approximation model of the diode.



. Offset diode model (0.7 Volt model)

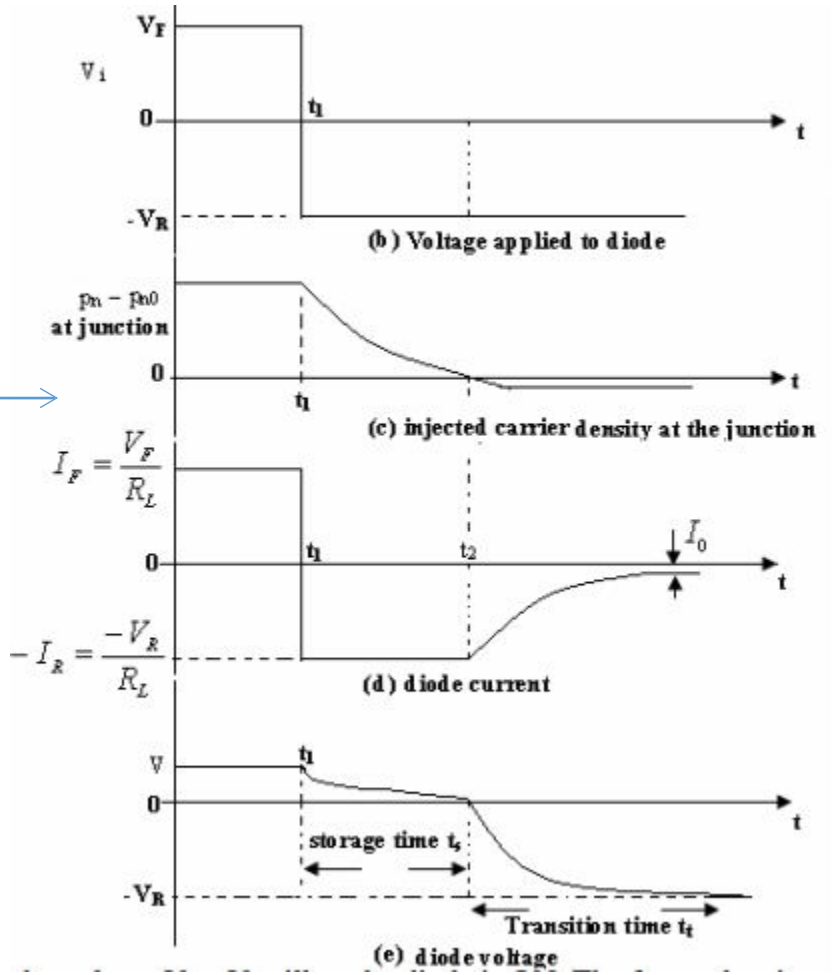
Contd….


I
V


1.0E-11
8.0E-12
6.0E-12
4.0E-12
2.0E-12
0.0E+0
-1.0E-12
Id (A)
reverse bias current
-0.4
-0.3
-0.2
-0.1
0.0
0.1
0.2
0.3
0.4
0.5
Vd (Volts)

Diode Switching times

- Reverse recovery time of the diode
- Forward recovery time of the diode

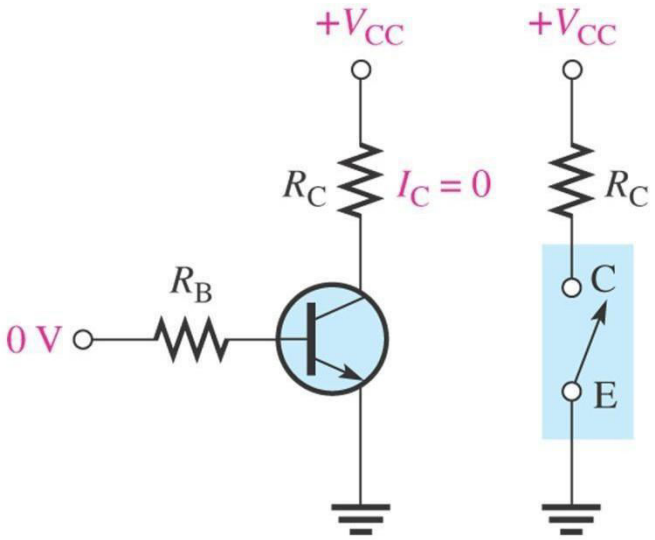


Contd…

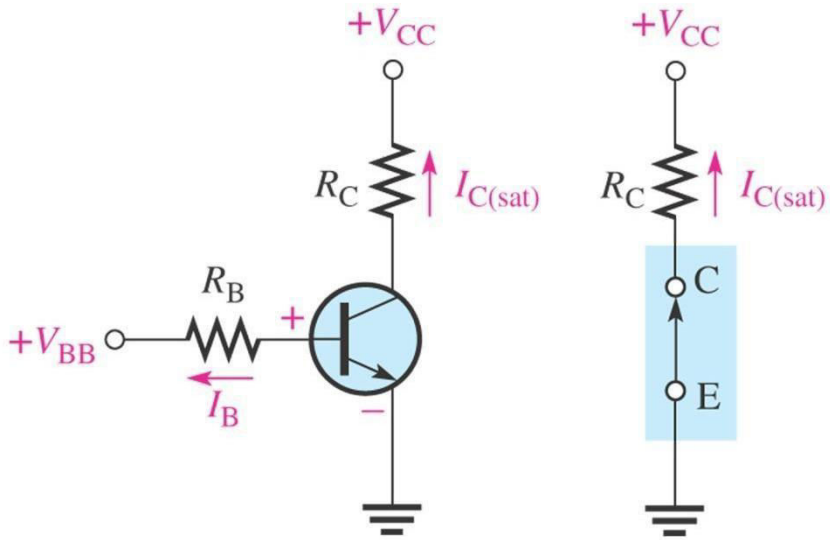
- As long as the voltage Vi = VF till t1, the diode is ON. The forward resistance of the diode being negligible when compared to RL, therefore If= Vf/R. At t = t1, the polarity of Vi is abruptly reversed, i.e.Vi = -VR and Ir = -Vr/R until t = t2 at which time minority carrier density pn at x = 0 has reached the equilibrium value pn0.
- At t = t2 the charge carriers have been swept, the polarity of the diode voltage reverses, the diode current starts to decrease. The time duration, t1 to t2, during which period the stored minority charge becomes zero is called the storage time ts. The time interval from t2 to the instant that the diode has recovered (V = -VR) is called the transition time,tt. The sum total of the storage time,ts and the transition time,tt is called the reverse recovery time of the diode, trr.
- trr = ts + tt

The BJT as a Switch

- Transistor as a Switch works in two regions
- Cut off
- Saturation

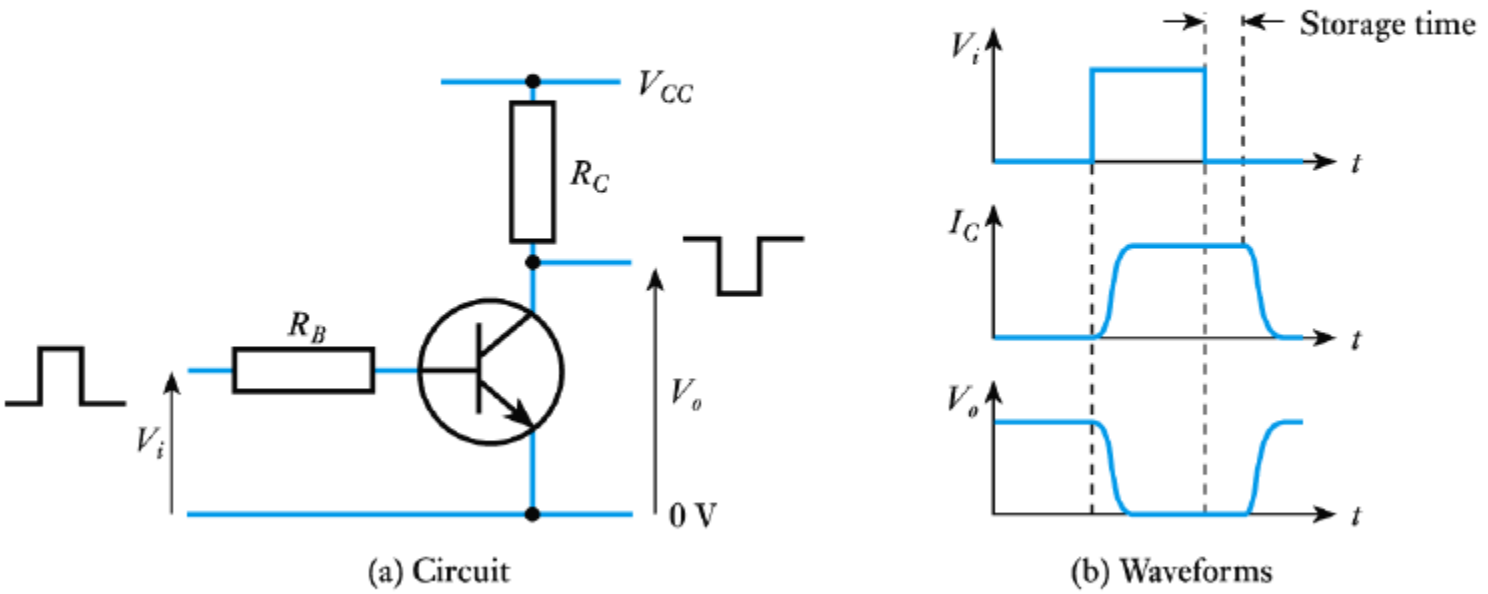


(a) Cutoff — open switch



(b) Saturation — closed switch

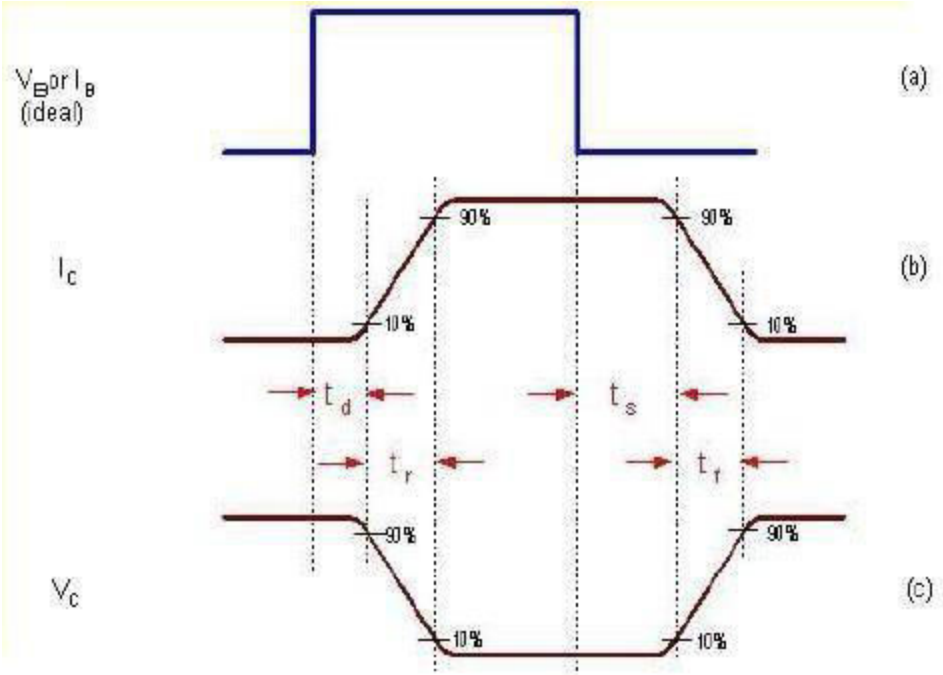
- **The bipolar transistor as a logical switch**



OHT 25.12

Transistor Switching Times

- Delay time(td)
- Rise time(tr)
- Storage time(ts)
- Fall time(tf)



Contd..

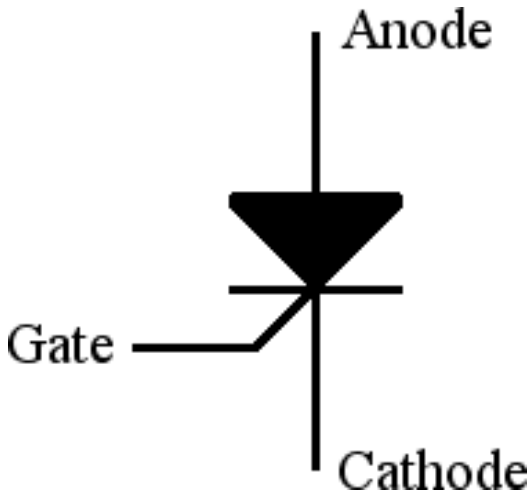
- **Delay Time, td** : It is the time taken for the collector current to reach from its initial value to 10% of its final value If the rise of the collector current is linear, the time required to rise to 10%IC(sat) is 1/8 the time required for the current to rise from 10% to 90% IC(sat). where tr is the rise time
- **Rise Time,tr** : It is the time taken for the collector current to reach from 10% of its final value to 90% of its final value. However, because of the stored charges, the current remains unaltered for sometime interval ts1 and then begins to fall. The time taken for this current to fall from its initial value at ts1 to 90% of its initial value is ts2. The sum of these ts1 and ts2 is approximately ts1 and is called the storage time.
- **Storage time, ts** : It is the time taken for the collector current to fall from its initial value to 90% of its initial value.
- **. Fall time, tf** : It is the time taken for the collector current to fall from 90% of its initial value to 10% of its Initial value.
- Ton= td+tr
- Toff= ts+tf

Breakdown mechanisms in BJTs

- The breakdown voltage of a BJT also depends on the chosen circuit configuration:
- In a common base mode (i.e. operation where the base is grounded and forms the common electrode between the emitter-base input and collector-base output of the device) the breakdown resembles that of a p-n diode.
- In a common emitter mode (i.e. operation where the emitter is grounded and forms the common electrode between the base-emitter input and the collector-emitter output of the device) the transistor action further influences the *I-V characteristics and breakdown voltage.*
- Avalanche breakdown of the base-collector junction is further influenced by transistor action in common-emitter mode of operation, since the holes generated by impact ionization are pulled back into the base region which results in an additional base current. This additional base current causes an even larger additional flow of electrons through the base and into the collector due to the current gain of the BJT. This larger flow of electrons in the base collector junction causes an even larger generation of electron-hole pairs.

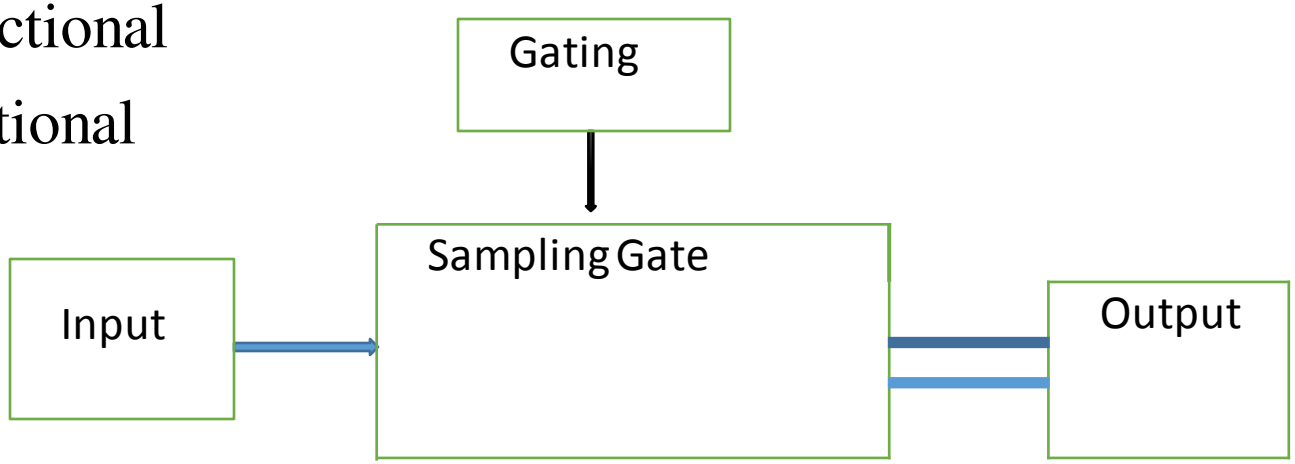
SCR

- A **S**ilicon **C**ontrolled **R**ectifier (or **S**emiconductor **C**ontrolled **R**ectifier) is a four layer solid state device that controls current flow
- The name "silicon controlled rectifier" is a trade name for the type of **thyristor** commercialized at General Electric in 1957



Sampling Gates

- Sampling Gates are also called as Transmission gates ,linear gates and selection circuits,in which the output is exact reproduction of the input during a selected time interval and zero otherwise.
- It has two inputs – gating signal, rectangular wave
- Two types
- Unidirectional
- Bidirectional



Principle of operation of a linear gate:

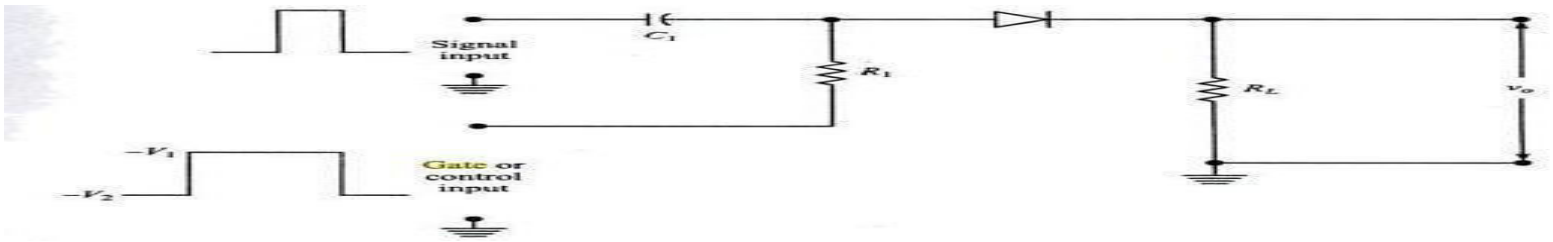
- Principle of operation of a linear gate: Linear gates can use (a) a series switch or (b) a shunt switch fig

Fig. Linear gates

In (a) the switch closes for transmitting the signal whereas in (b) the switch is open for transmission to take place.

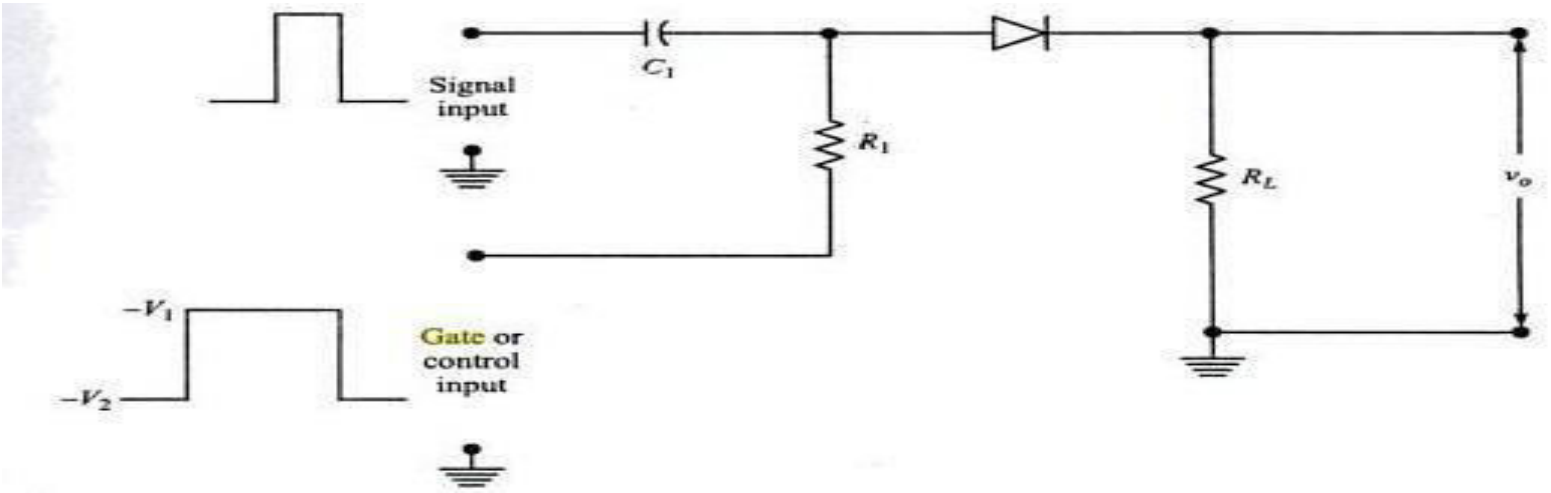
Unidirectional Gate

- unidirectional sampling gates are those which transmit signals of only one polarity(i.e,. either positive or negative)
- The gating signal is also known as control pulse, selector pulse or an enabling pulse. It is a negative signal, the magnitude of which changes abruptly between –V2 and –V1.



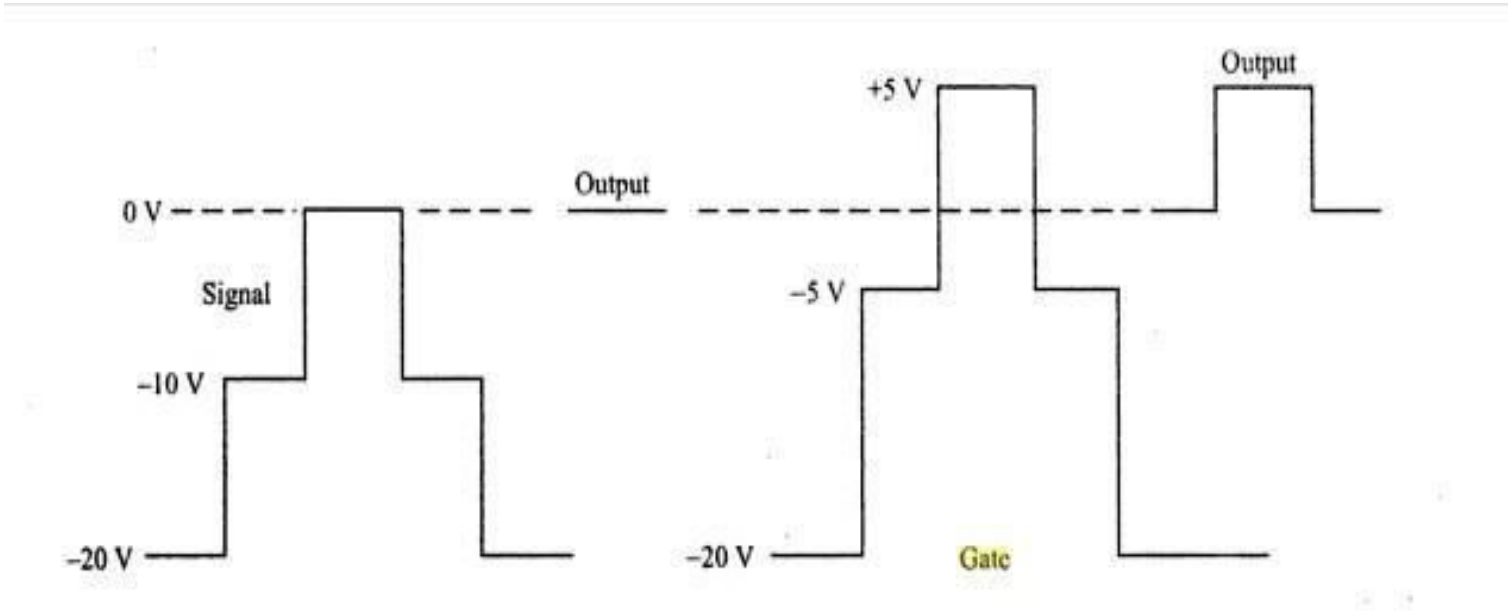
Unidirectional gate

- Consider the instant at which the gate signal is –V1 which is a reasonably large negative voltage. Even if an input pulse is present at this time instant, the diode remains OFF as the input pulse amplitude may not be sufficiently large so as to forward bias it. Hence there is no output. Now consider the duration when the gate signal has a value –V2 and when the input is also present (coincidence occurs).



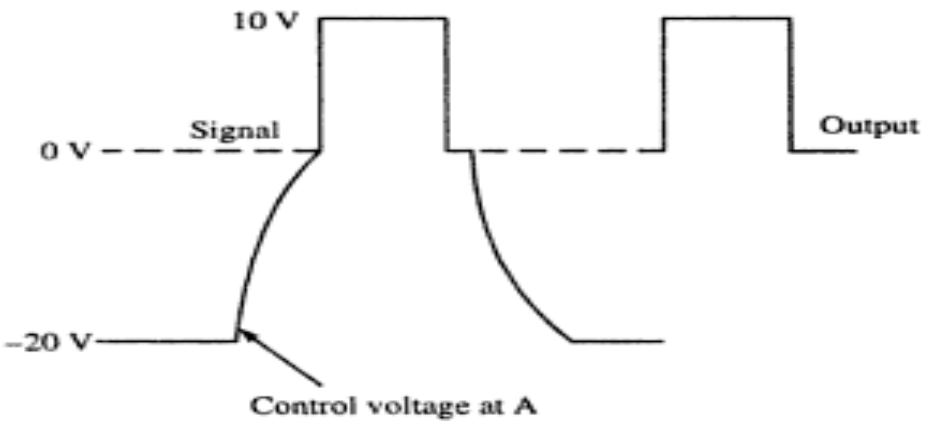
Output waveform

- When the control signal shifted to upward



pedesta
l

- When the control signal is shifted to positive value ,so it will be superimposed on input and control signals .so the pedestal occurs



Unidirectional diode coincidence gate

- When any of the control voltages is at –V1, point X is at a large negative voltage, even if the input pulse Vs is present., D0 is reverse biased. Hence there is no signal at the output.
- When all the control voltages, on the other hand, are at –V2 , if an input signal Vs is present, D0 is forward biased and the output is a pulse of 5V. Hence this circuit is a coincidence circuit or AND circuit.

A unidirectional diode coincidence gate is shown below.

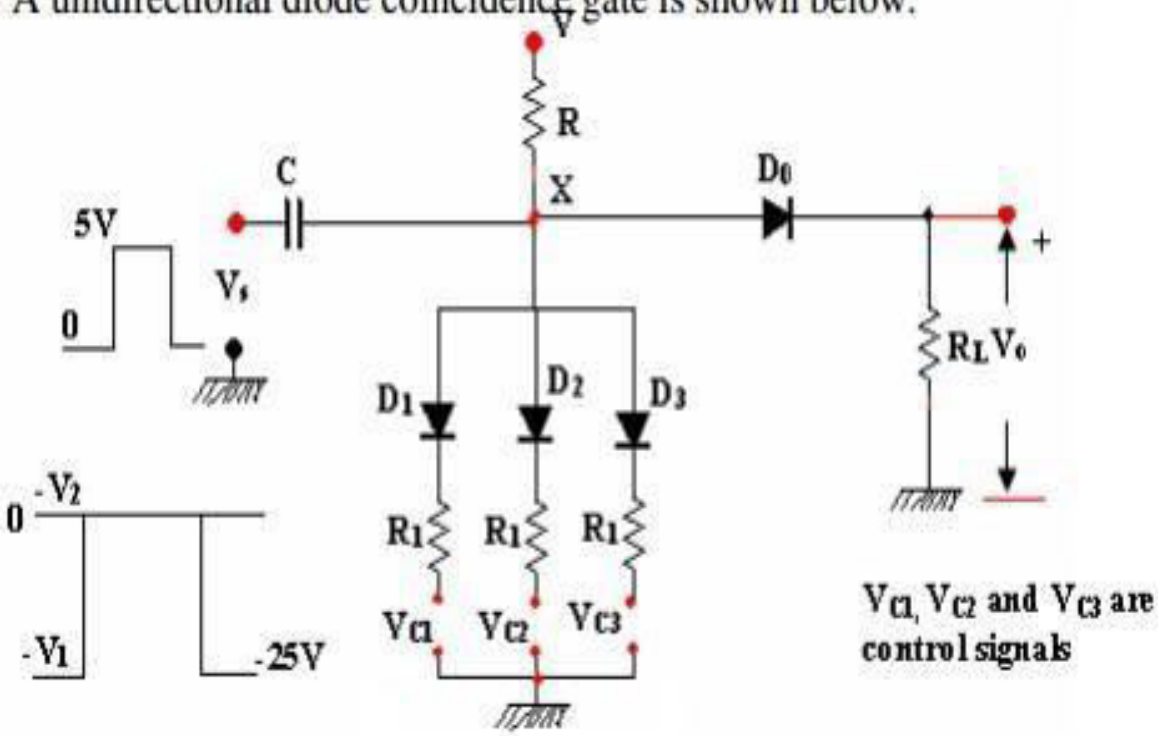
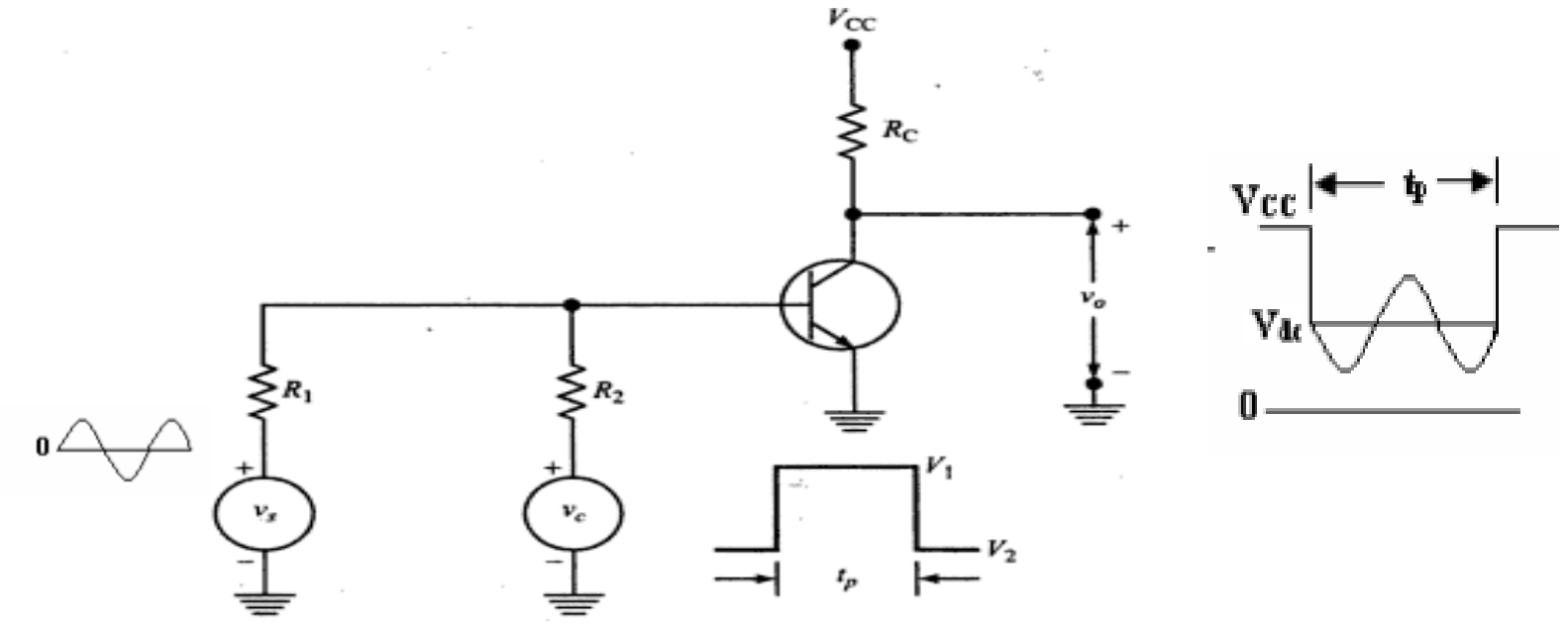


Fig. A unidirectional diode AND gate

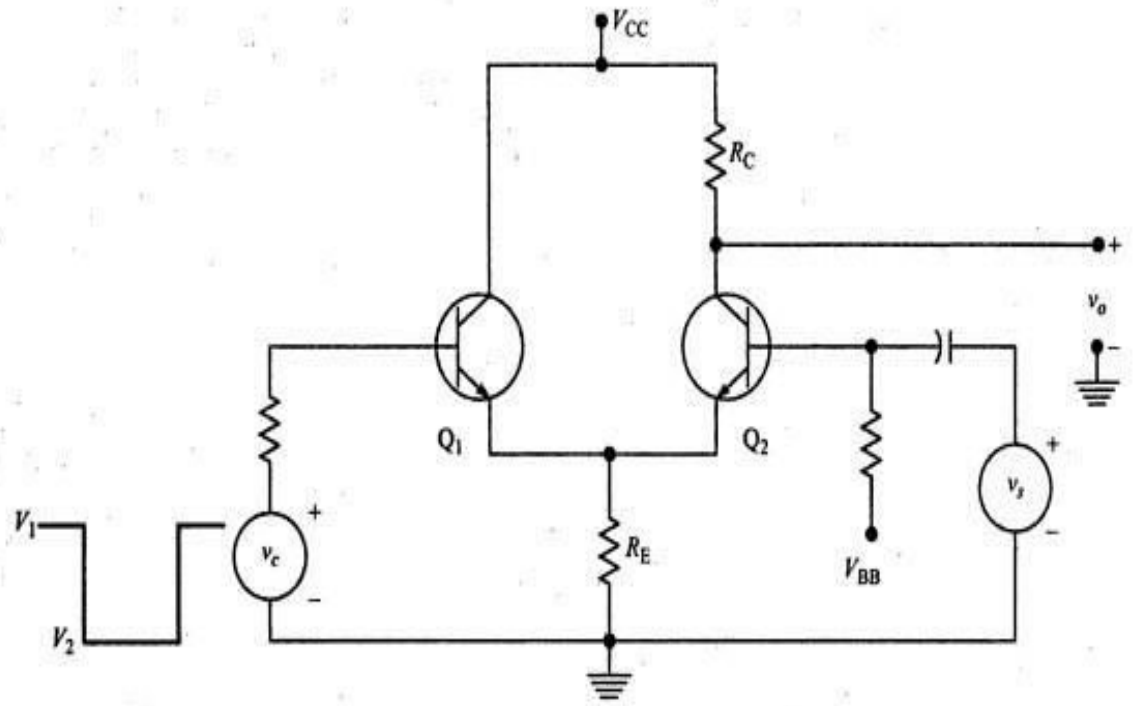
Bidirectional Sampling gate

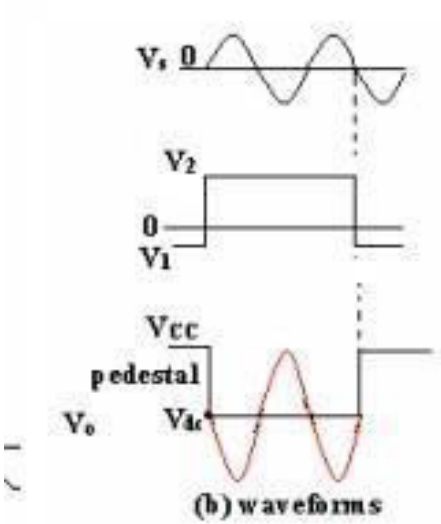
- Bidirectional sampling gates are those which transmit signals of both the polarities.



Bidirectional Sampling gate using Transistor

- Bidirectional sampling gates are those which transmit signals of both the polarities.

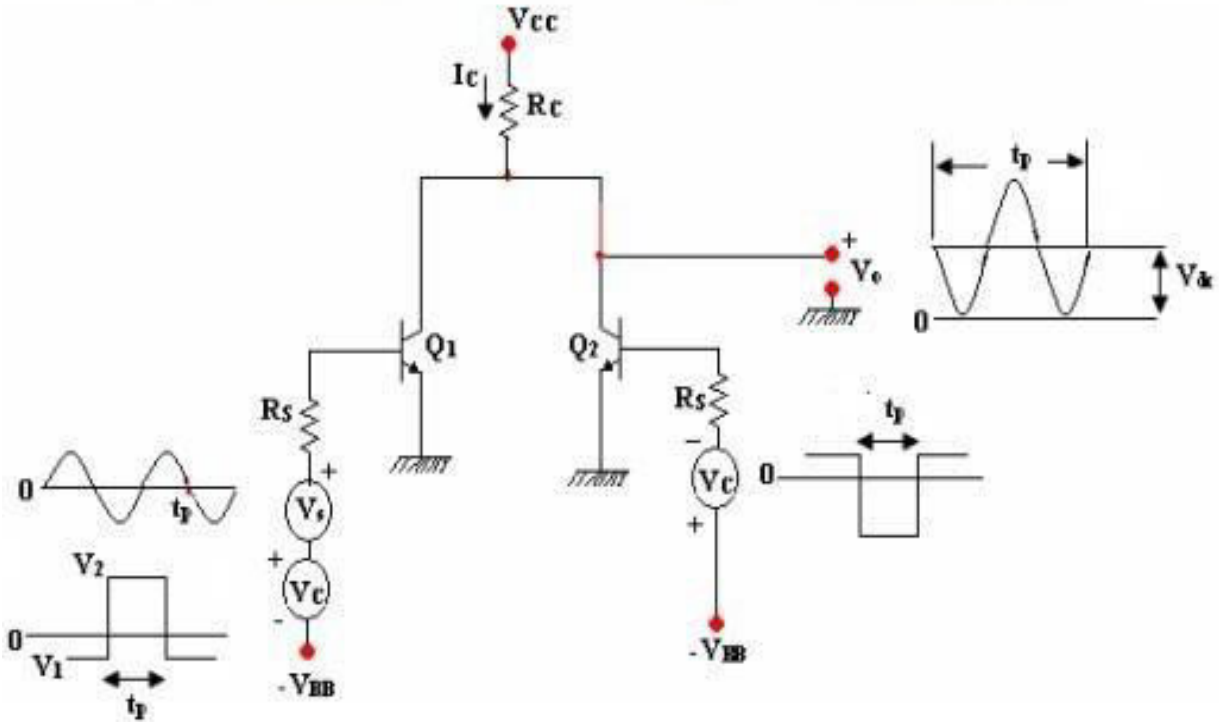




Circuit that minimizes the pedestal

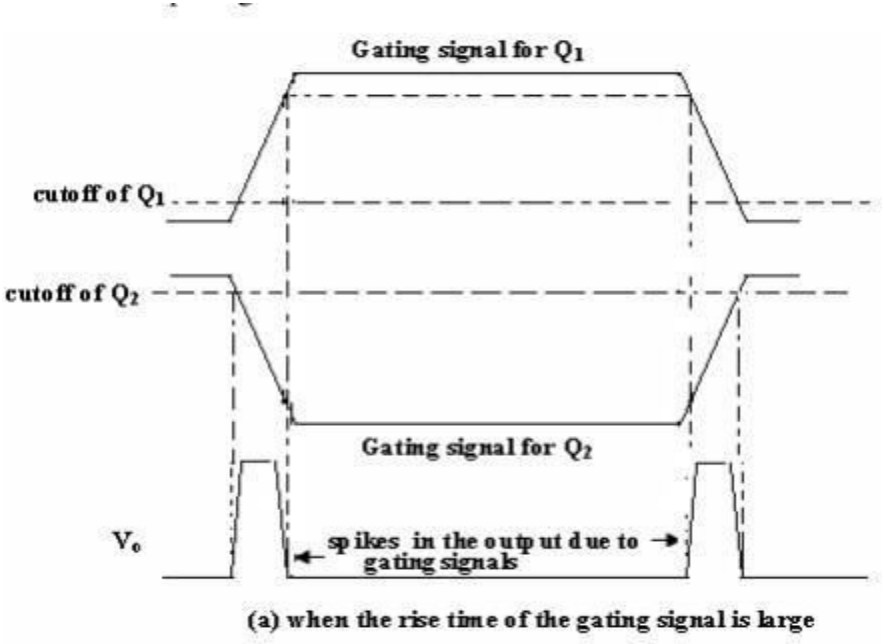
- Circuit that minimizes the pedestal

A circuit arrangement that reduces this pedestal is shown in fig.



Contd …

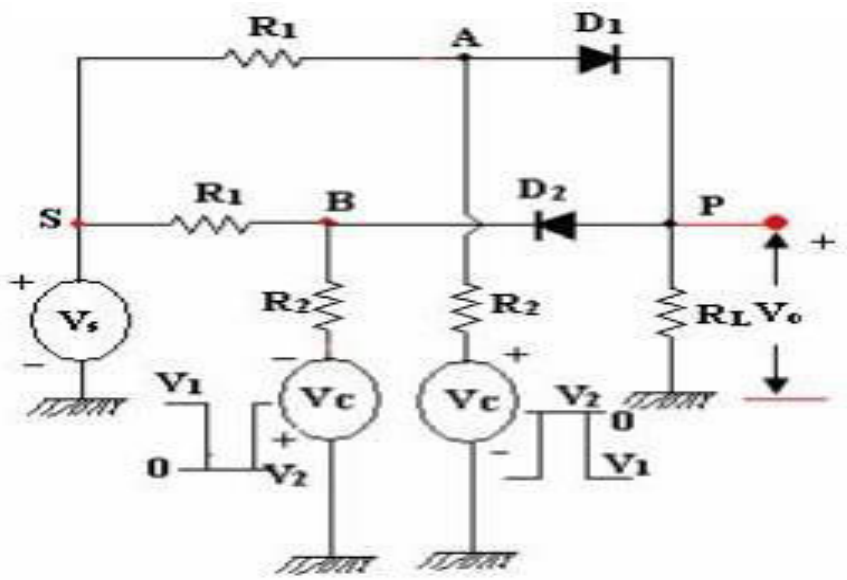
- The control signal applied to the base of Q2 is of opposite polarity to that applied to the base of Q1. When the gating signal connected to Q1 is negative, Q1 is OFF and at the same time the gating signal connected to Q2 drives Q2 ON and draws current IC. As a result there is a dc voltage Vdc at the collector. But when the gate voltage at the base of Q1 drives Q1 ON, Q2 goes OFF. But during this gate period if the input signal is present, it is amplified and is available at the output, with phase inversion. But the dc reference level practically is Vdc. As such the pedestal is either eliminated or minimized.



(a) when the rise time of the gating signal is large

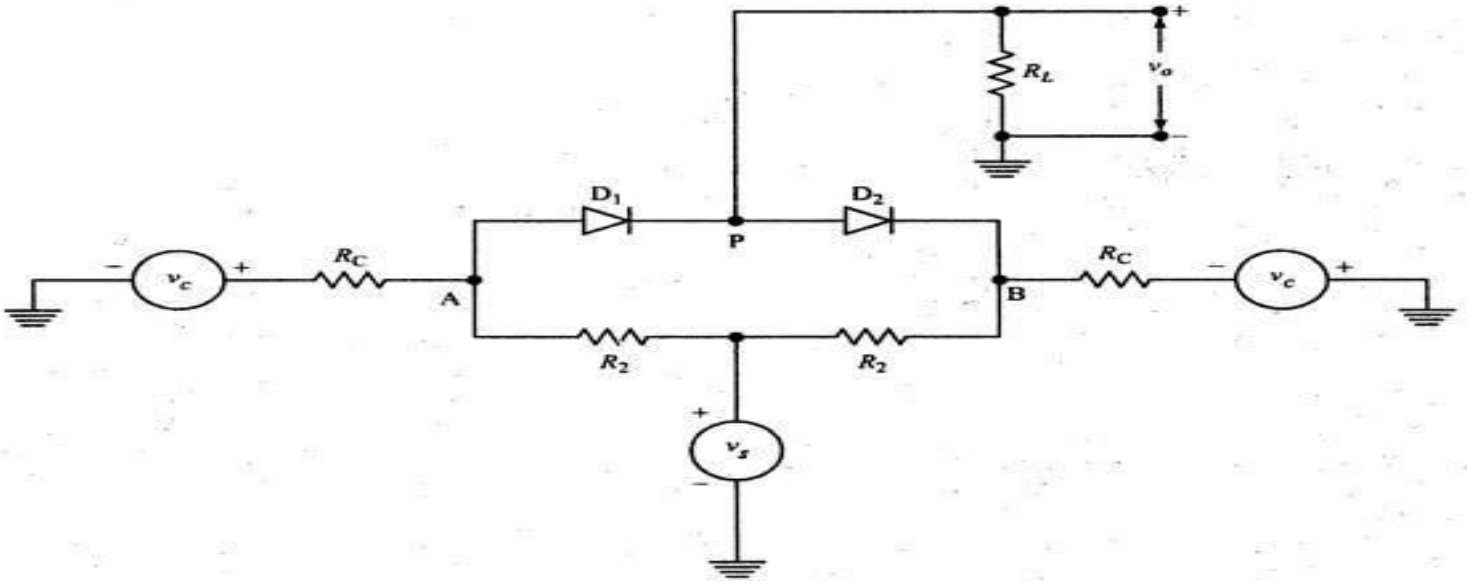
Two Diode Sampling gate

- When the control signals are at V1, D1 and D2 are OFF, no input signal is transmitted to the output. But when control signals are at V2, diode D1 conducts if the input is positive pulses and diode D2 conducts if the input is negative pulses. Hence these bidirectional inputs are transmitted to the output. This arrangement eliminates pedestal, because of the circuit symmetry.



Four Diode Sampling gate

- When the control signals are at V1, D1 and D2 are OFF, no input signal is transmitted to the output. But when control signals are at V2, diode D1 conducts if the input is positive pulses and diode D2 conducts if the input is negative pulses. Hence these bidirectional inputs are transmitted to the output. This arrangement eliminates pedestal, because of the circuit symmetry.

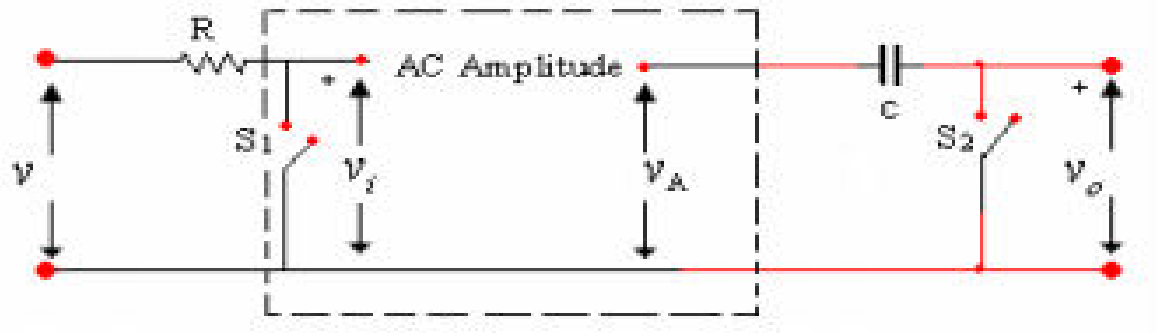


Applications

- Chopper Amplifier
- Multiplexers
- ADC
- Sampling Scope
- Sample and hold circuits

Chopper Amplifier

- Sometimes it becomes necessary to amplify a signal v that has very small dv/dt and that the amplitude of the signal itself is very small, typically of the order of millivolts. Neither, ac amplifiers using large coupling condensers nor dc amplifiers with the associated drift would be useful for such an application. A chopper stabilized amplifier employing sampling gates can be a useful choice in such a applications



Chopper stabilized amplifier

UNIT -4

MULTIVIBRATORS

and

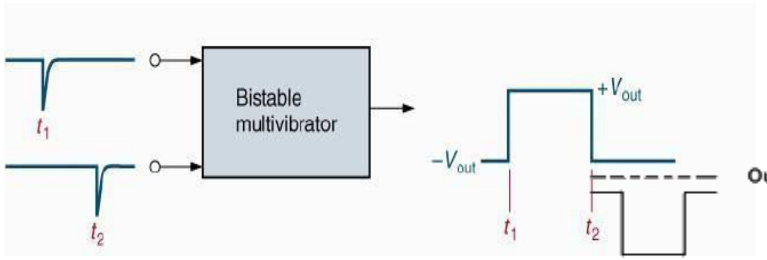
TIME BASE GENERATORS

Multivibrators

- Multivibrator – A circuit designed to have zero, one, or two stable output states.
- There are three types of multivibrators.
  - Astable (or Free-Running Multivibrator)
  - Monostable (or One-Shot)
  - Bistable (or Flip-Flop)

Bistable Multivibrators

- Bistable multivibrator – A switching circuit with two stable output states. The bistable multivibrator has two absolutely stable states
  - Also referred to as a flip-flop.
  - The output changes state when it receives a valid input trigger signal, and remains in that state until another valid trigger signal is received.



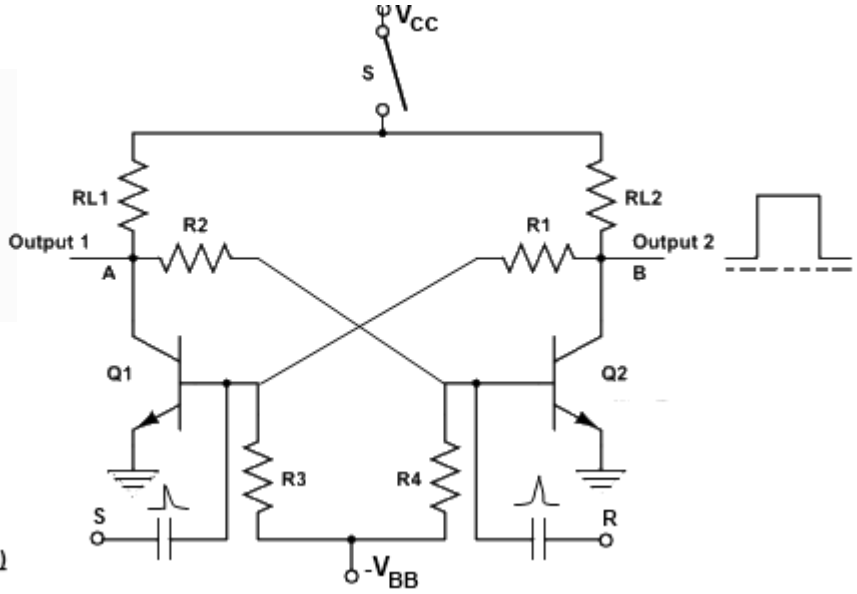
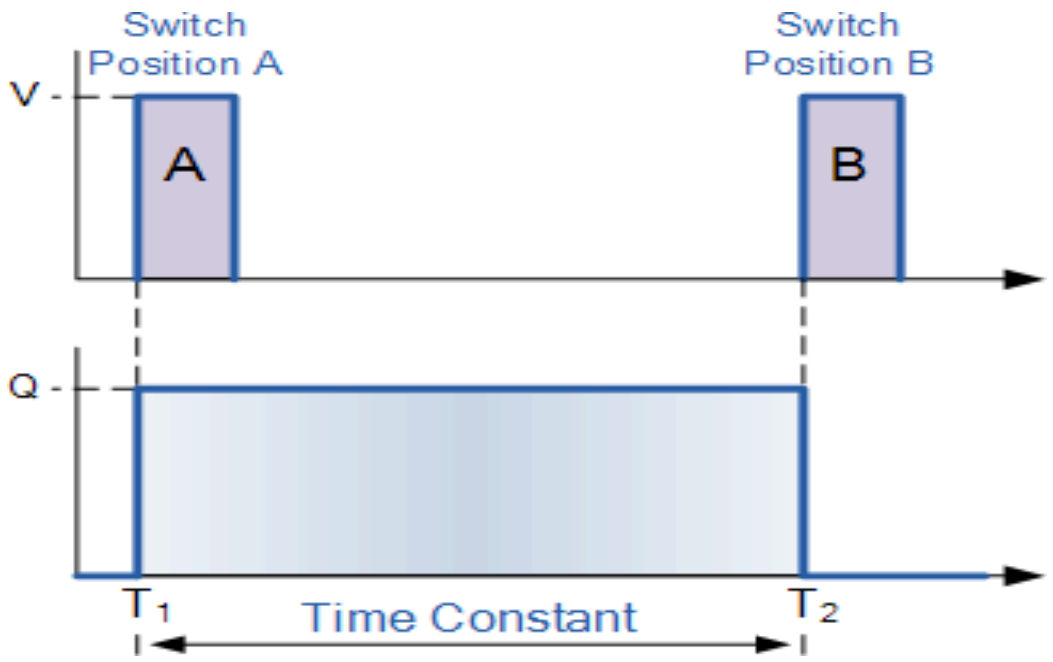


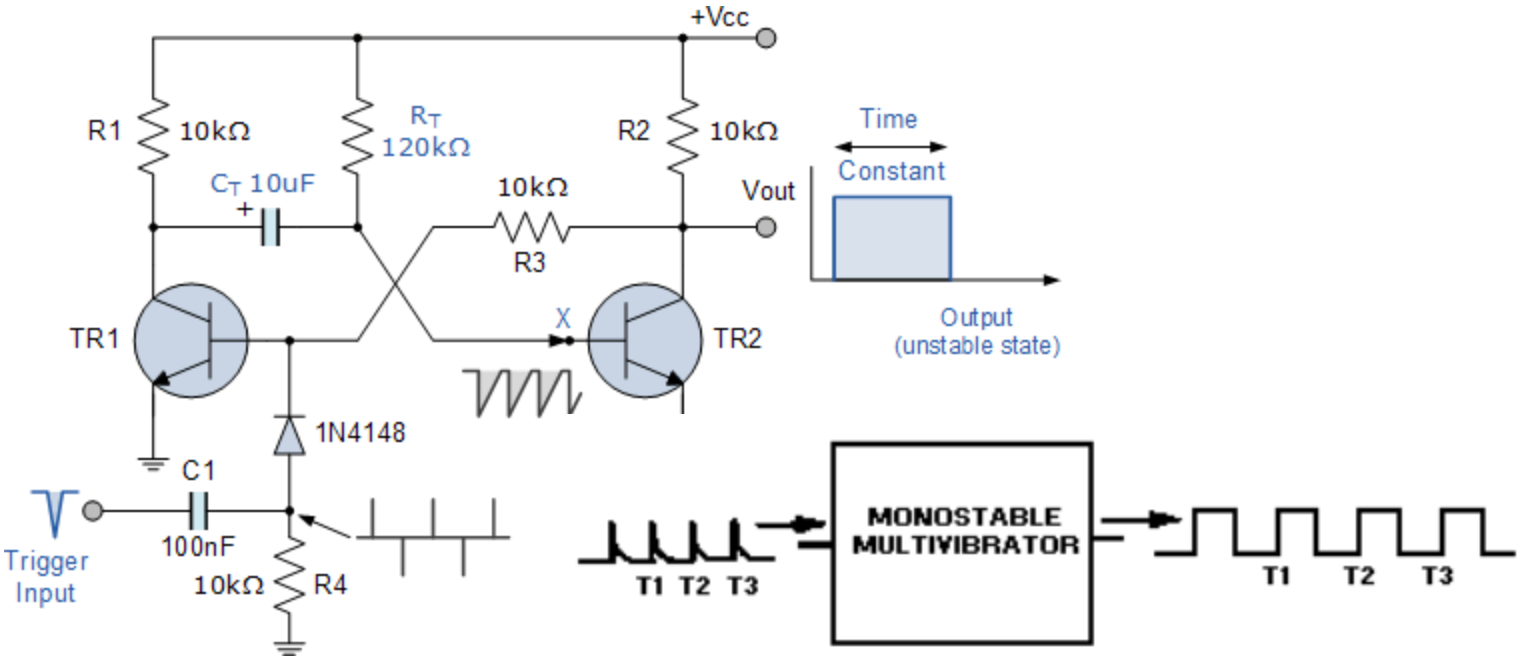
Figure (a)

Bistable Multivibrator Waveform

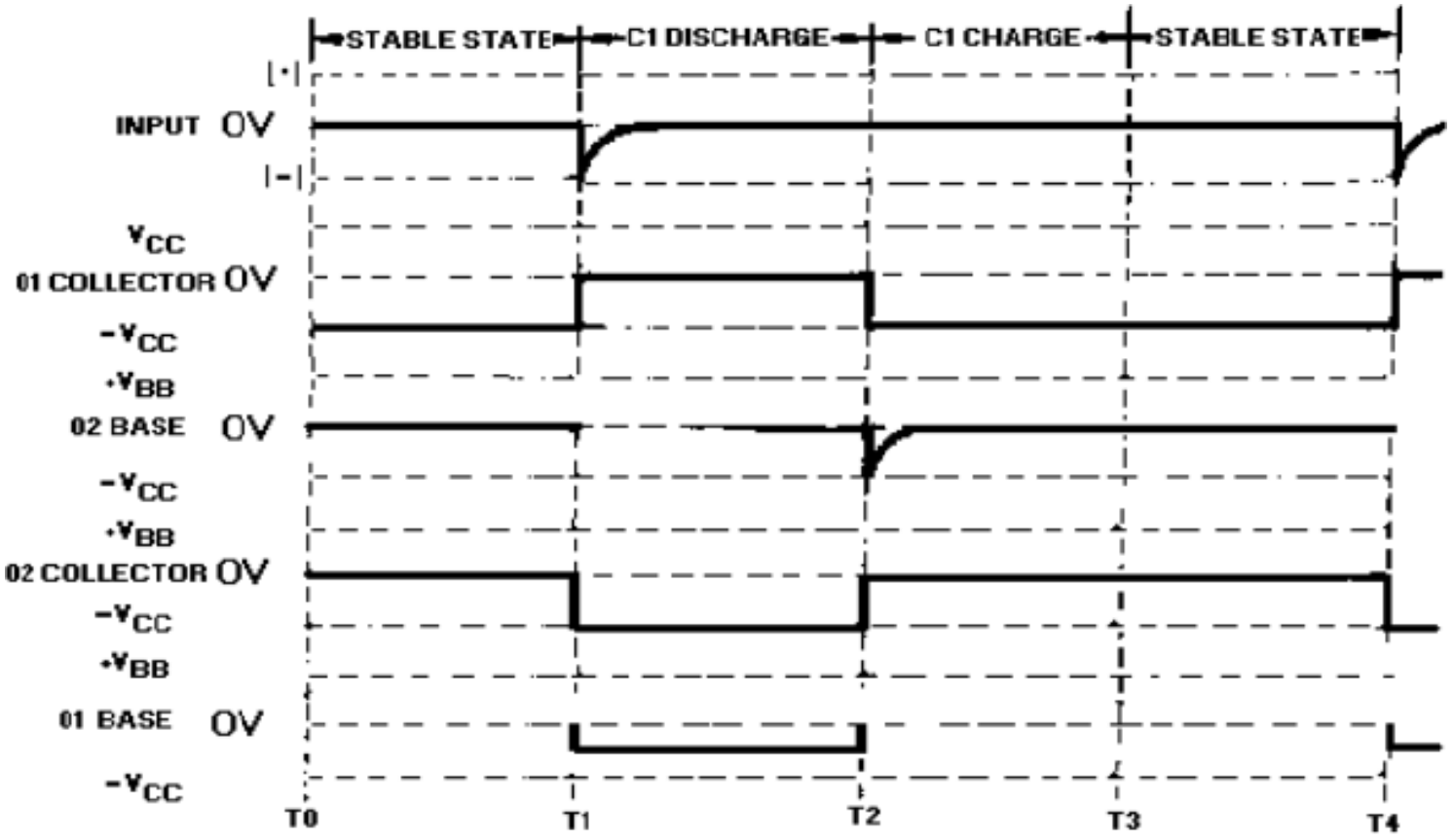


Monostable Multivibrator

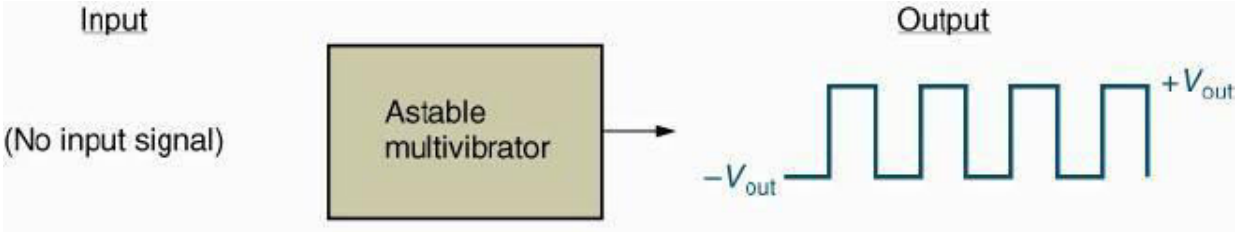
- Multivibrators have two different electrical states, an output "HIGH" state and an output "LOW" state giving them either a stable or quasi-stable state depending upon the type of multivibrator. One such type of a two state pulse generator configuration are called **Monostable Multivibrators**.
- **Monostable Multivibrators** have only **ONE** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable Multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

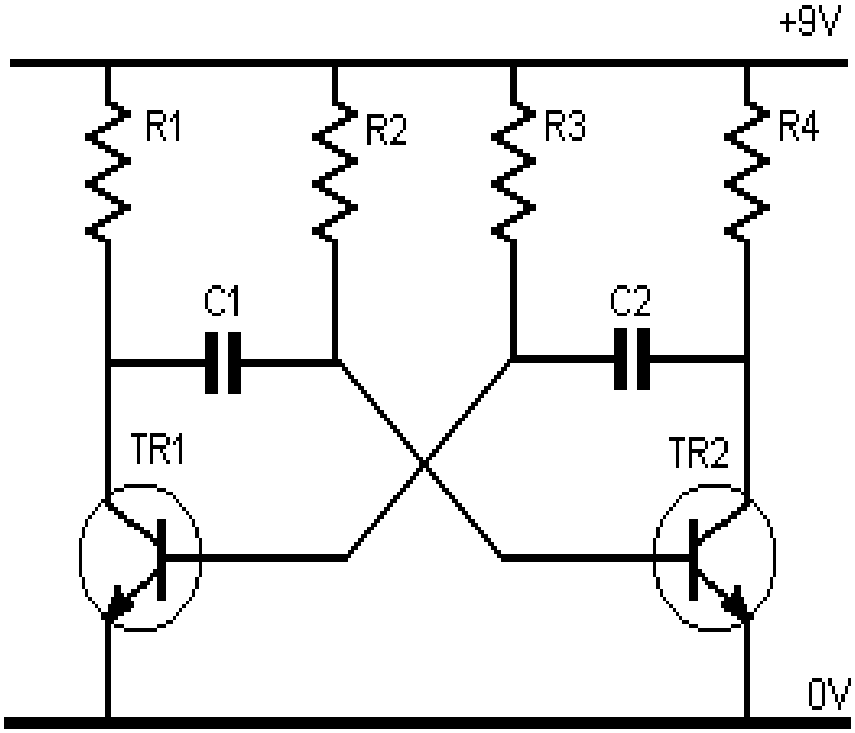


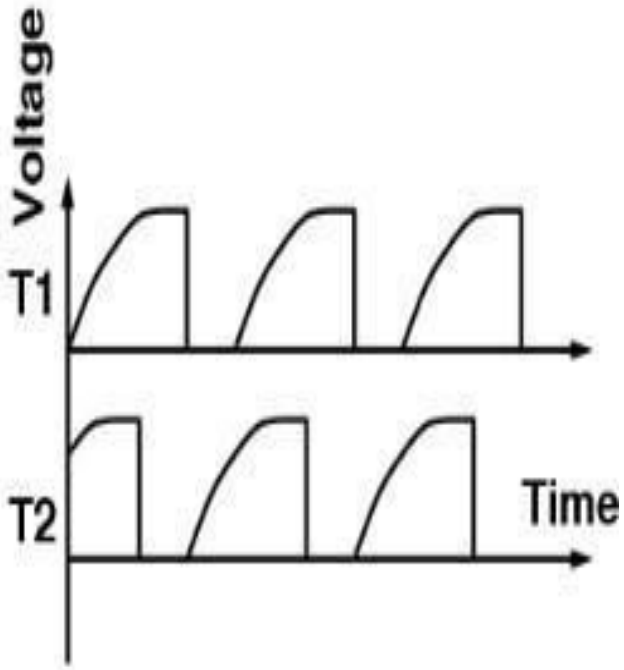
Waveforms


STABLE STATE
C1 DISCHARGE
C1 CHARGE
STABLE STATE
INPUT OV
+
-
+VCC
01 COLLECTOR OV
-VCC
+VBB
02 BASE OV
-VCC
+VBB
02 COLLECTOR OV
-VCC
+VBB
01 BASE OV
-VCC
T0
T1
T2
T3
T4

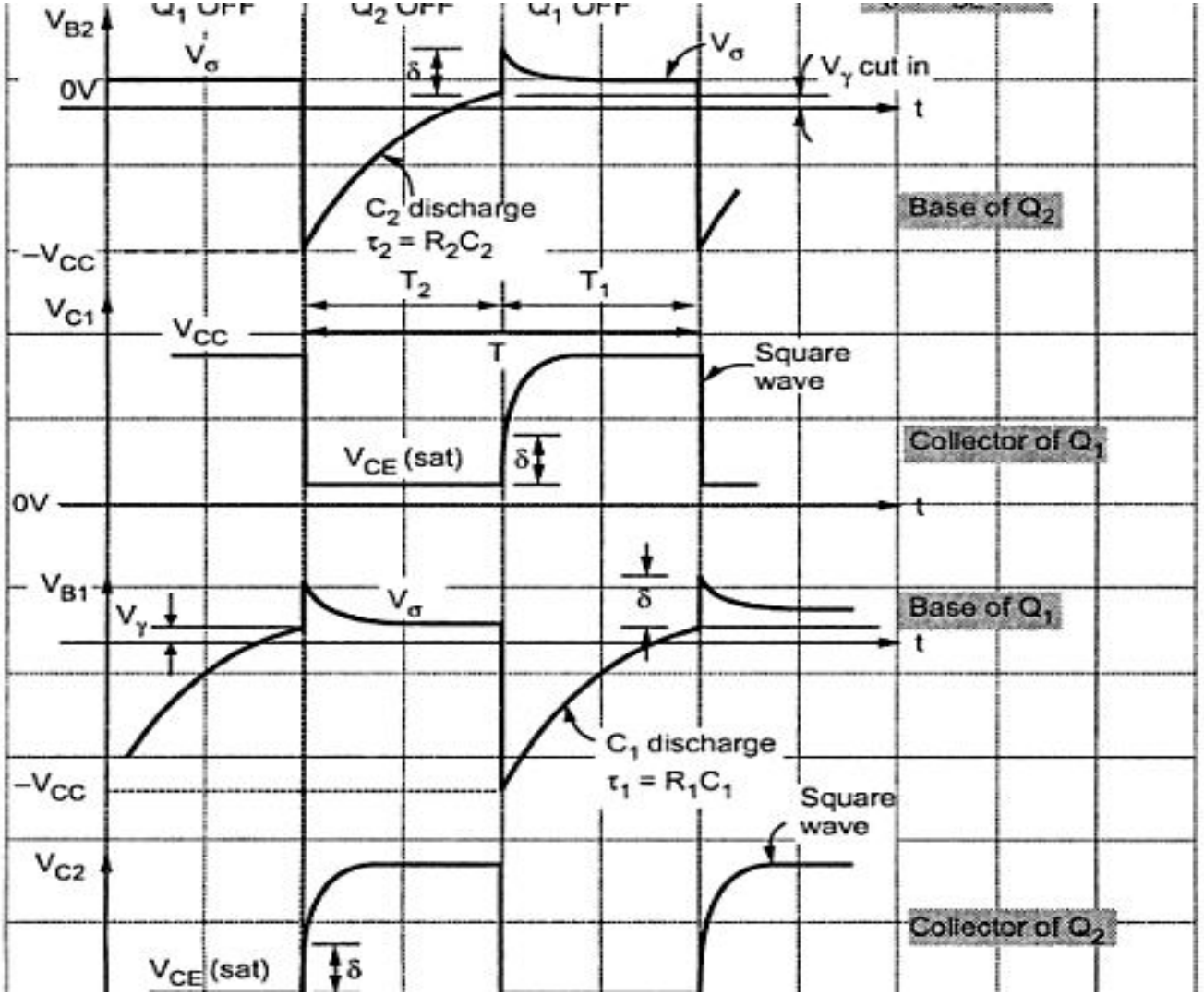
Astable Multivibrator



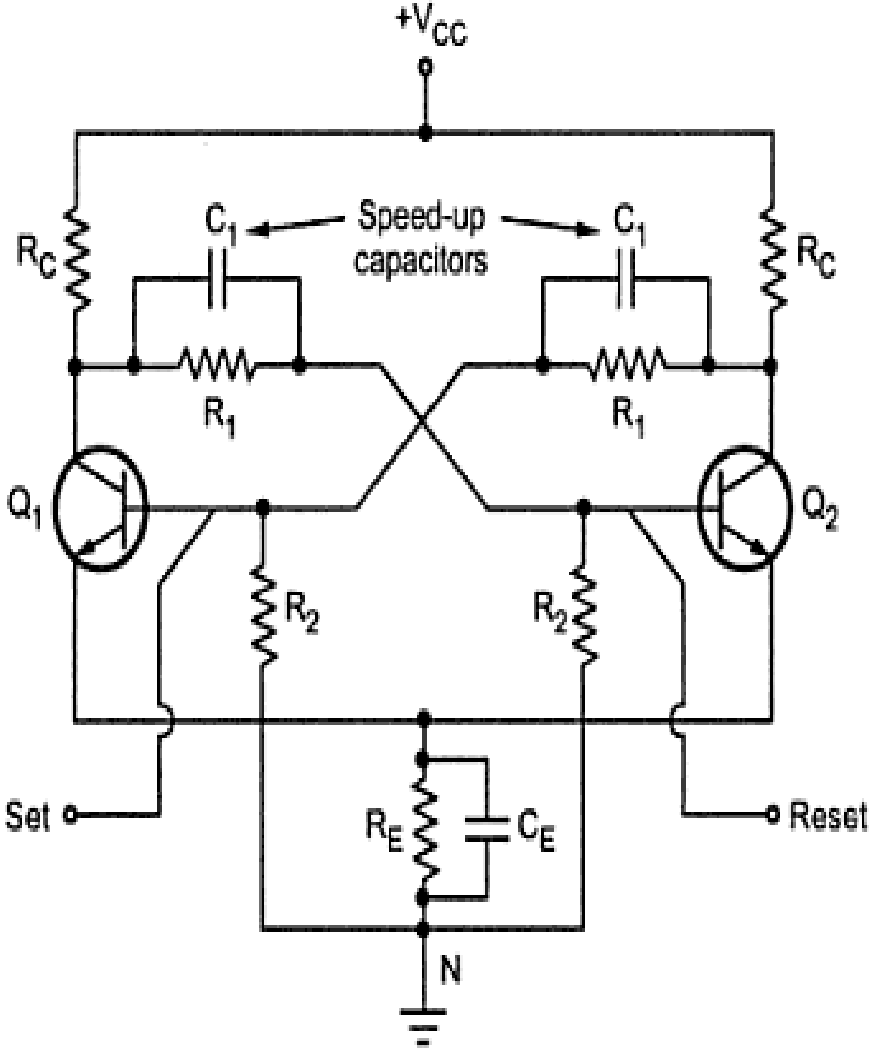




Waveforms


V_{B2}
Q_1 OFF
Q_2 OFF
Q_1 OFF
V_σ
δ
V_σ
V_γ cut in
0V
t
C_2 discharge
$\tau_2 = R_2C_2$
Base of Q_2
$-V_{CC}$
T_2
T_1
V_{C1}
V_{CC}
T
Square wave
V_{CE} (sat)
δ
Collector of Q_1
0V
t
V_{B1}
V_γ
V_σ
δ
Base of Q_1
t
C_1 discharge
$\tau_1 = R_1C_1$
$-V_{CC}$
Square wave
V_{C2}
Collector of Q_2
V_{CE} (sat)
δ

Commutating Capacitors



- Conduction transfers takes two phases
- 1) Transition time
- 2) Settling time

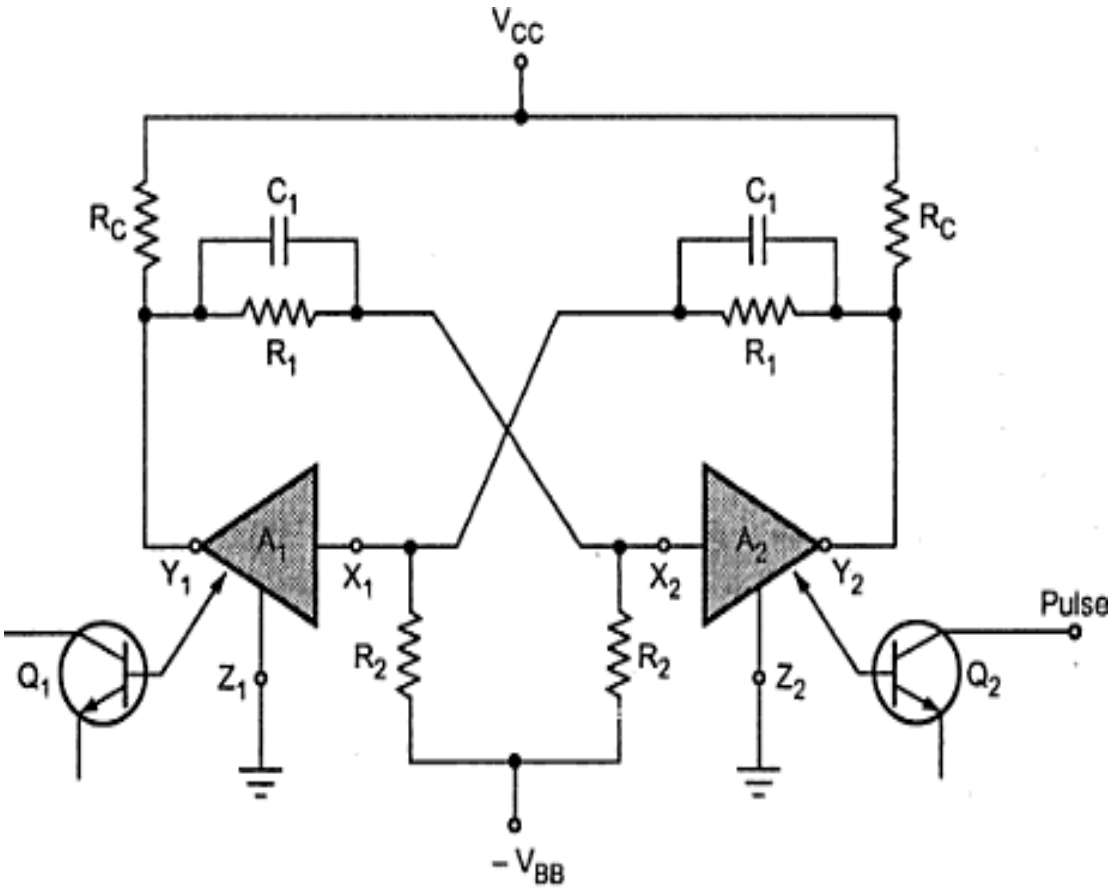
$$f_{max} = \frac{1}{2C_1(R_1 \| R_2)} = \frac{(R_1 + R_2)}{2C_1 R_1 R_2}$$

Triggering the binary

- Two types of triggering
- 1) Symmetrical 2) Unsymmetrical
- In un symmetrical triggering, two triggers are required. One to set the circuit in particular stable state and other is to reset

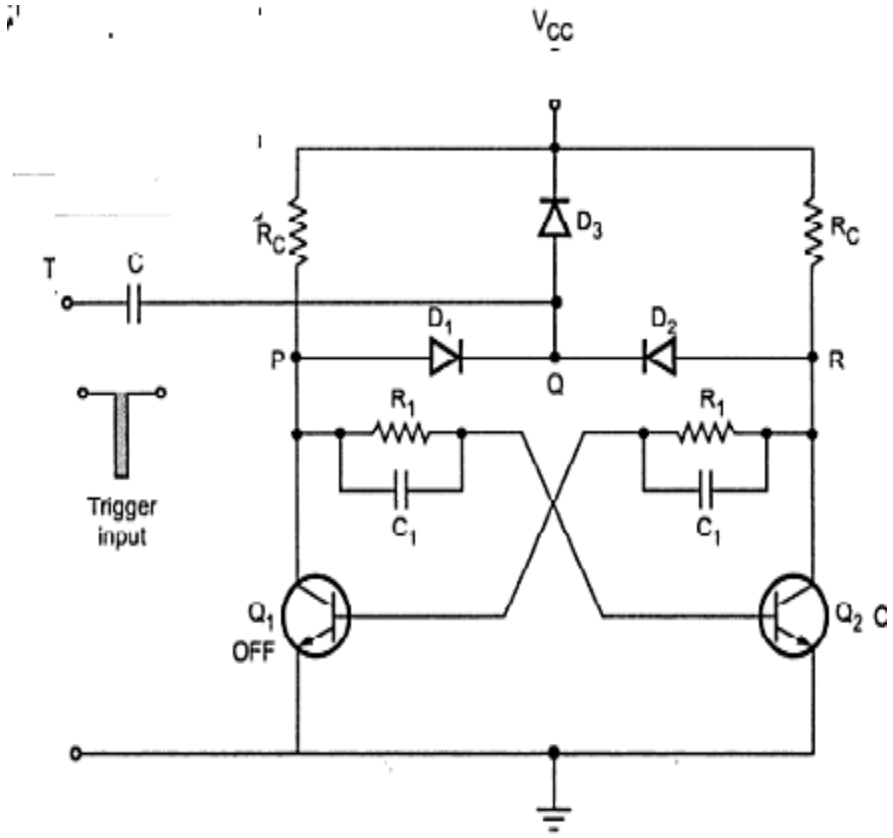
- In Symmetrical triggering , uses only one trigger pulse input to the any of the one transistor

Triggering the binary



- Unsymmetrical

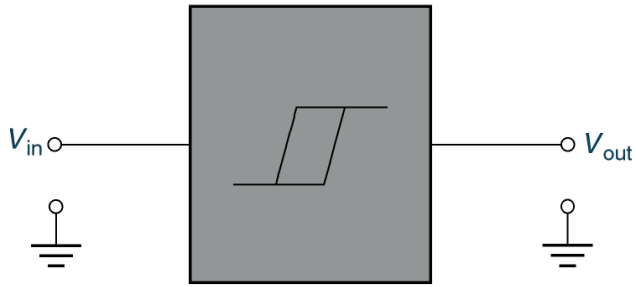
symmetrical

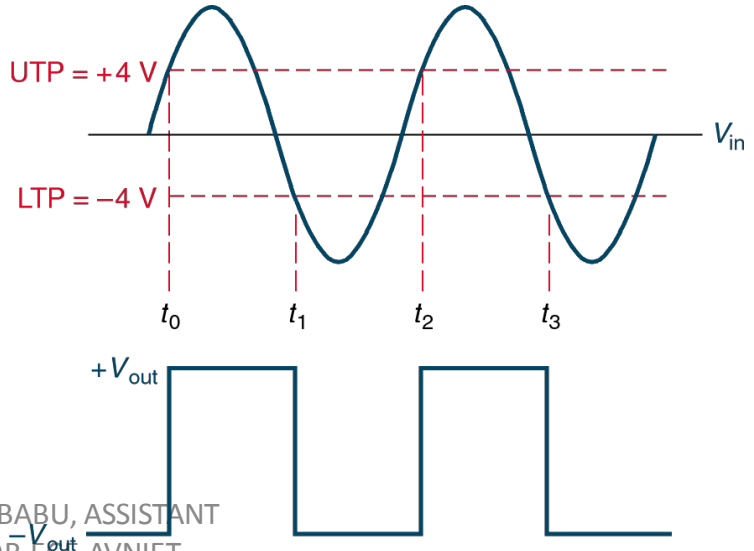


- symmetrical

Schmitt Triggers

- Schmitt trigger – A voltage-level detector.
- The output of a Schmitt trigger changes state when
  - When a positive-going input passes the upper trigger point (UTP) voltage.
  - When a negative-going input passes the lower trigger point (LTP) voltage.

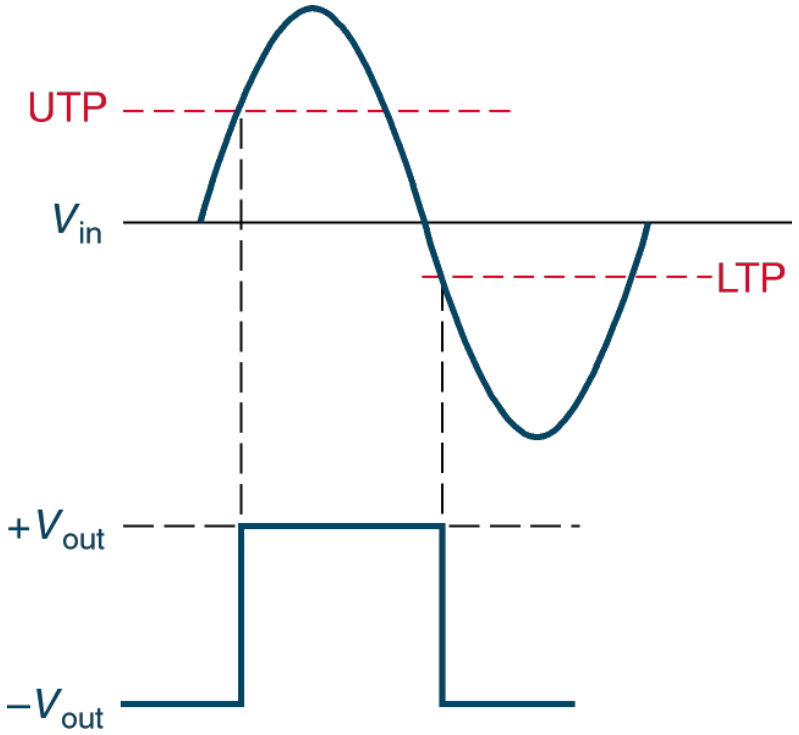




Note: The symbol shown in the block is commonly used to represent Schmitt trigger circuits.

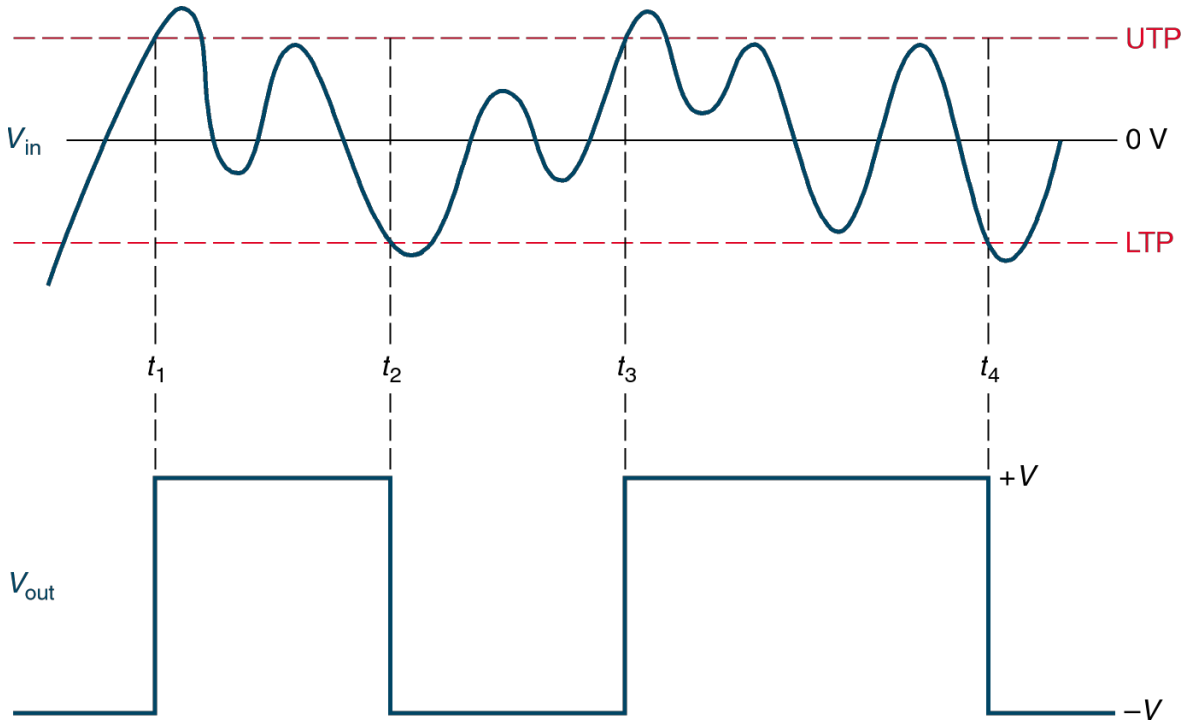
Trigger Point Voltages

- Trigger point voltages may be equal or unequal in magnitude, and are opposite in polarity.

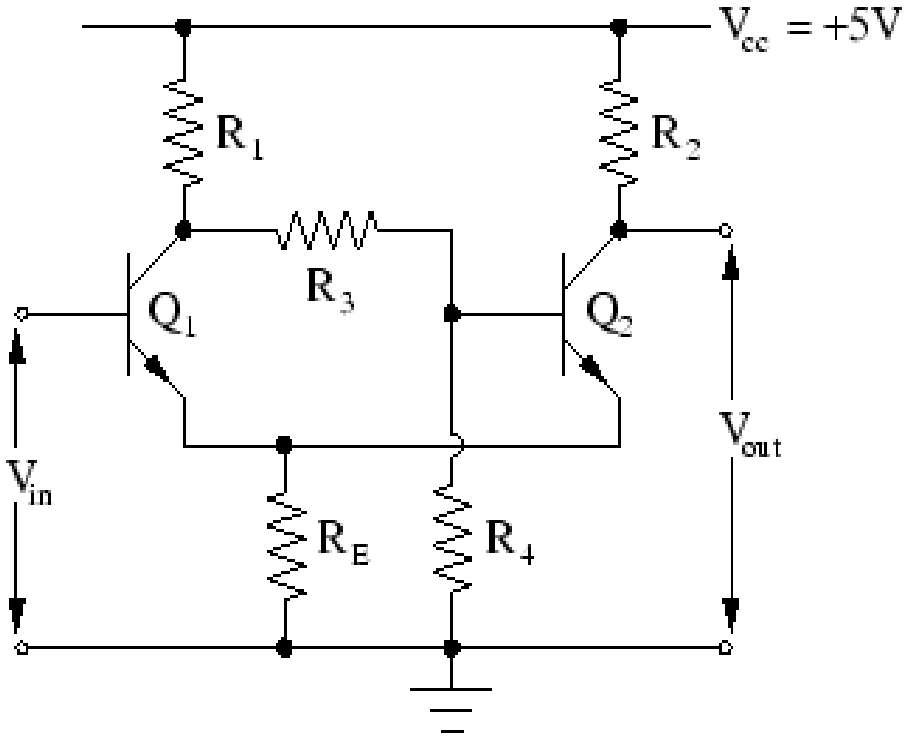


Hysteresis

- Hysteresis – A term that is often used to describe the range of voltages between the UTP and LTP of a Schmitt trigger.



Schmitt trigger using transister



Astable multivibrator to generate a square wave of 1 kHz:

$$h_{fe} = 25$$

- Assume NPN transistor with
- Let $I_c = 5mA$

$$V_{cc} = 12V$$

$$T_1 = T_2 = T/2$$

- Assume symmetrical square wave i.e.
- Neglect the junction voltages.
- We have f= 1 kHz
- So, T=1/1kHz = 1ms

- Let Q_2 ON and Q_1 OFF. Then

R_{c2}

$=(12-0)/\Omega 5$ R_{c1}

$=2.4k$ =

$$i_{B2(\min)} = \frac{C2(sat)}{h_{fe}}$$

$=5/25$

$=0.2\text{mA}$

Q_2

- Whe $i_{B2} = 1.5 x i_{B2}(\min)$ n:

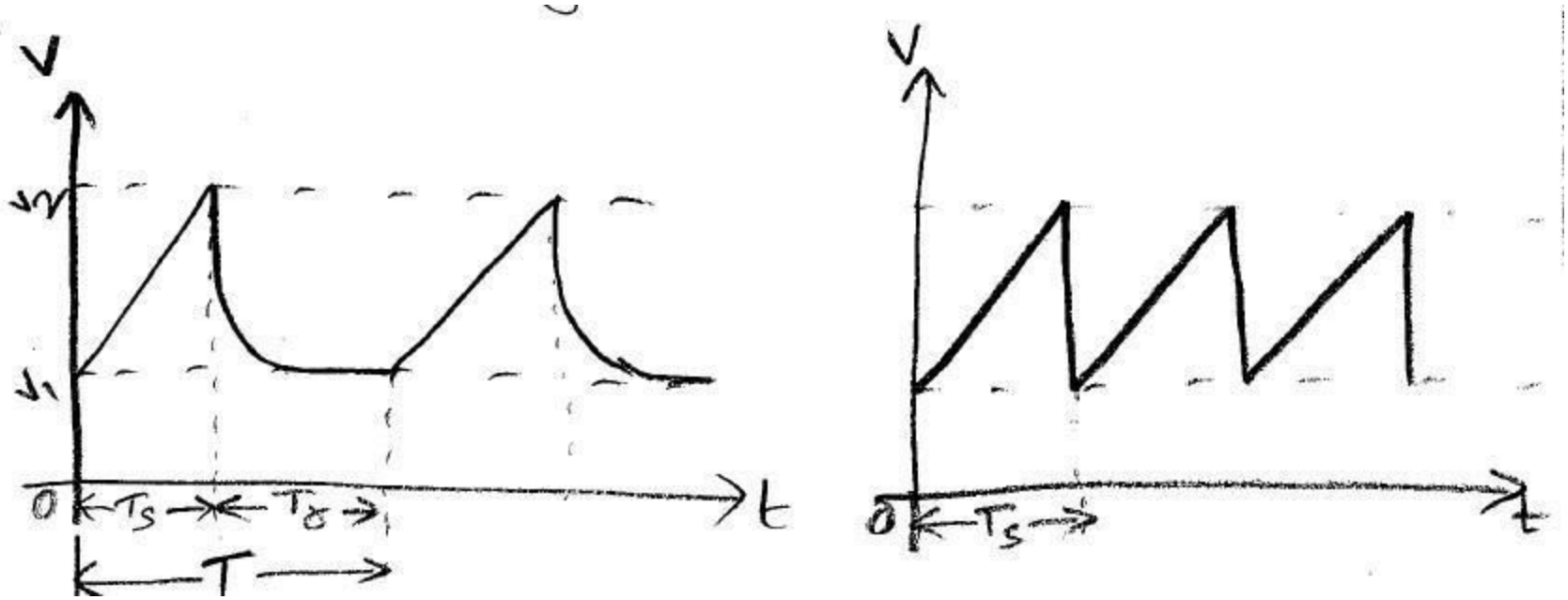
$$=1.5X0.2$$

$$=0.3mA$$

Applications

- Oscillator
- Timer
- Voltage –to- frequency converter
- Voltage controlled oscillator
- Clock source
- Square wave generator

General features of time base generator



Time base generator

Constant current charging

- A capacitor is charged with constant current source.
- As it charged with constant current, it is charged linearly.

Miller circuit:

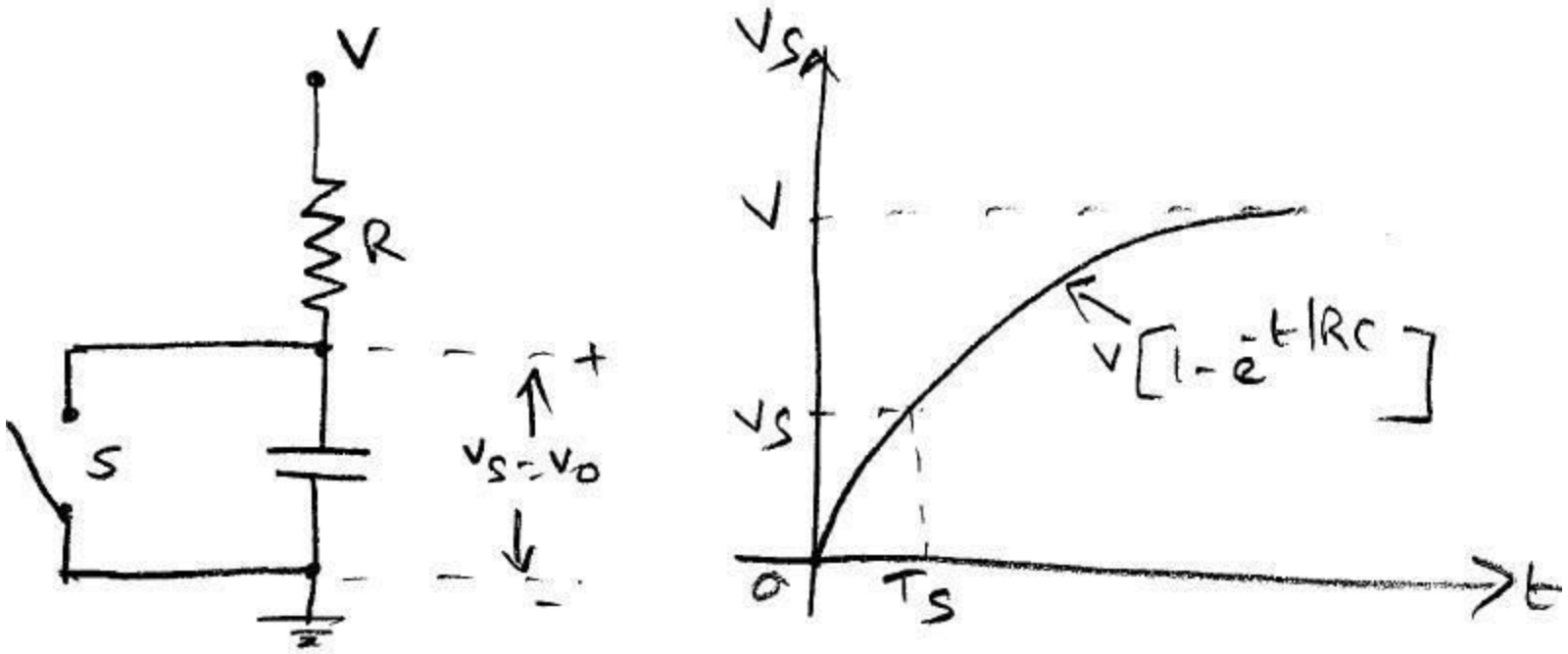
- Integrator is used to convert a step waveform to ramp waveform.

Bootstrap circuits

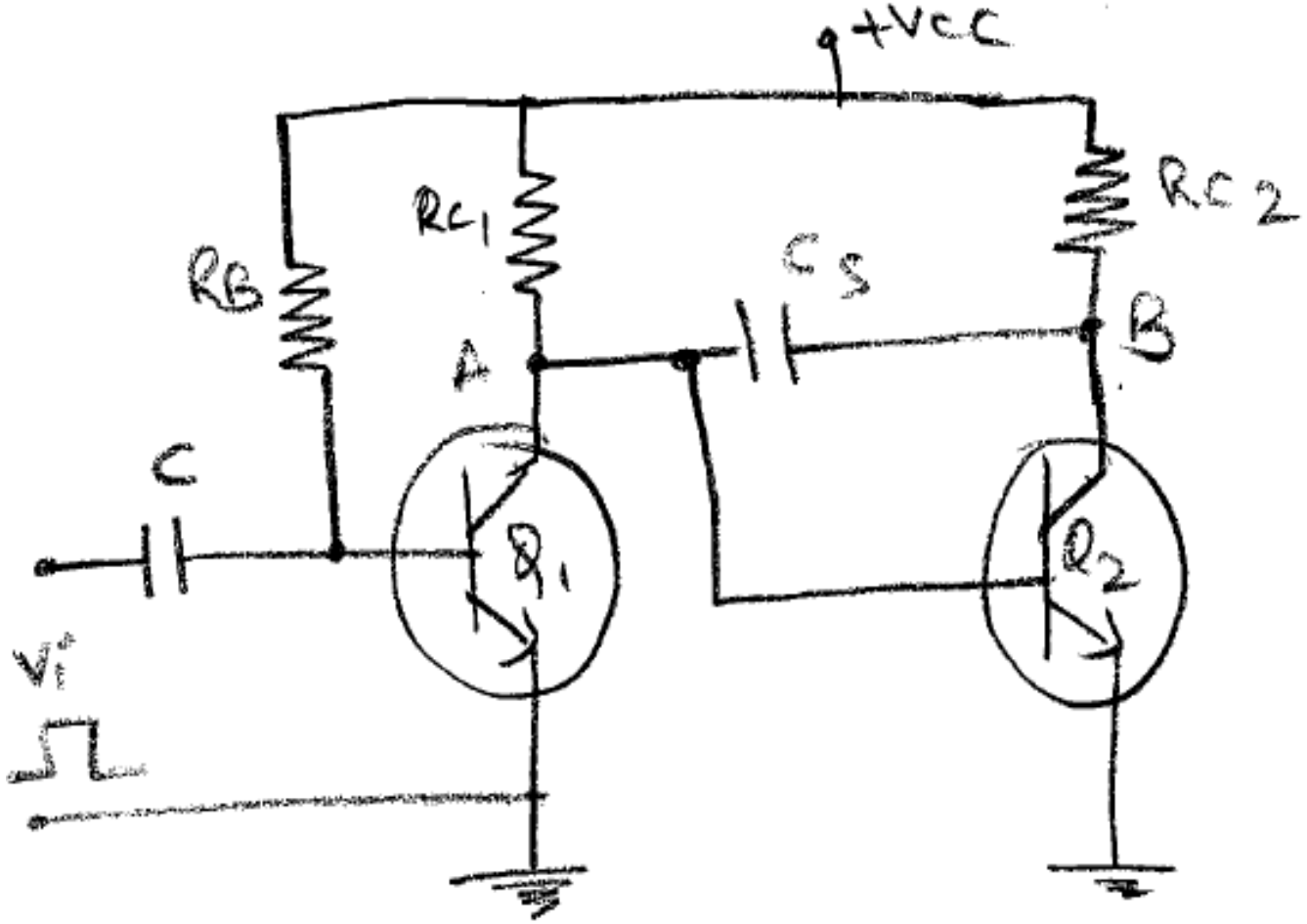
- A constant current source is obtained by maintaining nearly constant voltage across the fixed resistor in series with capacitor.

Compensating network is used to improve the linearity of bootstrap and miller time base generator

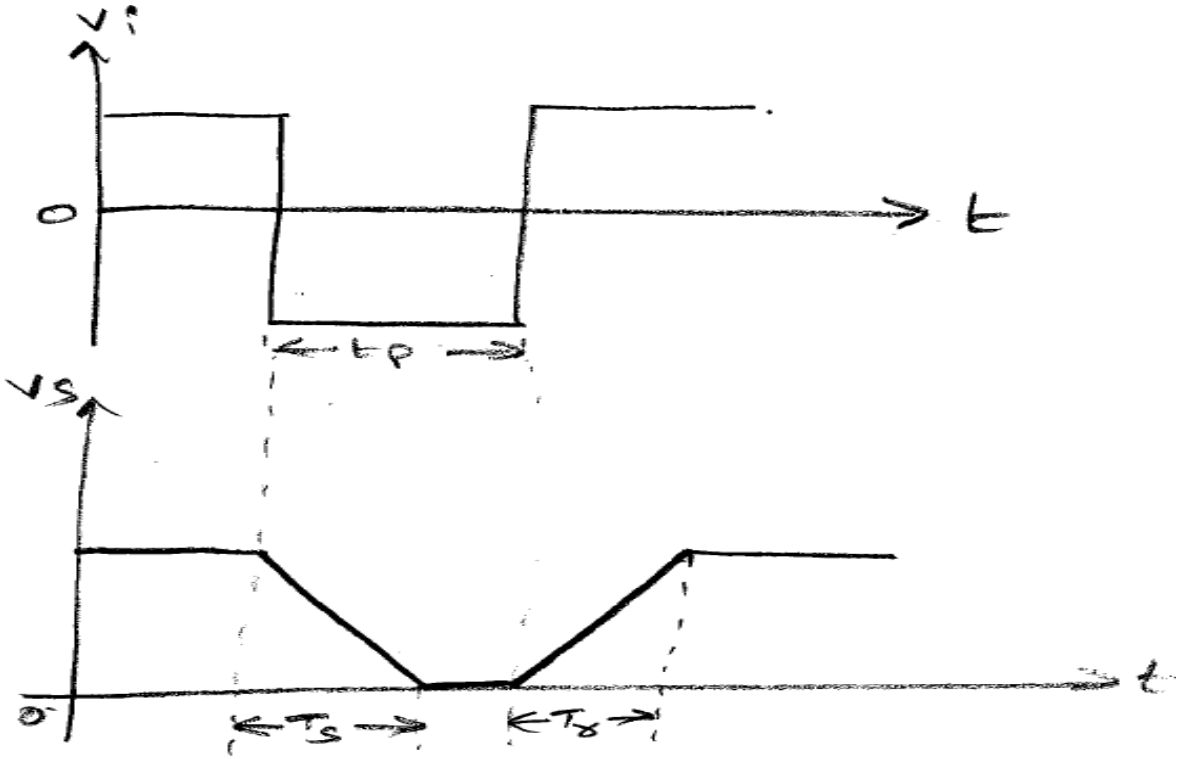
Exponential sweep circuit



Transistor miller time base generator

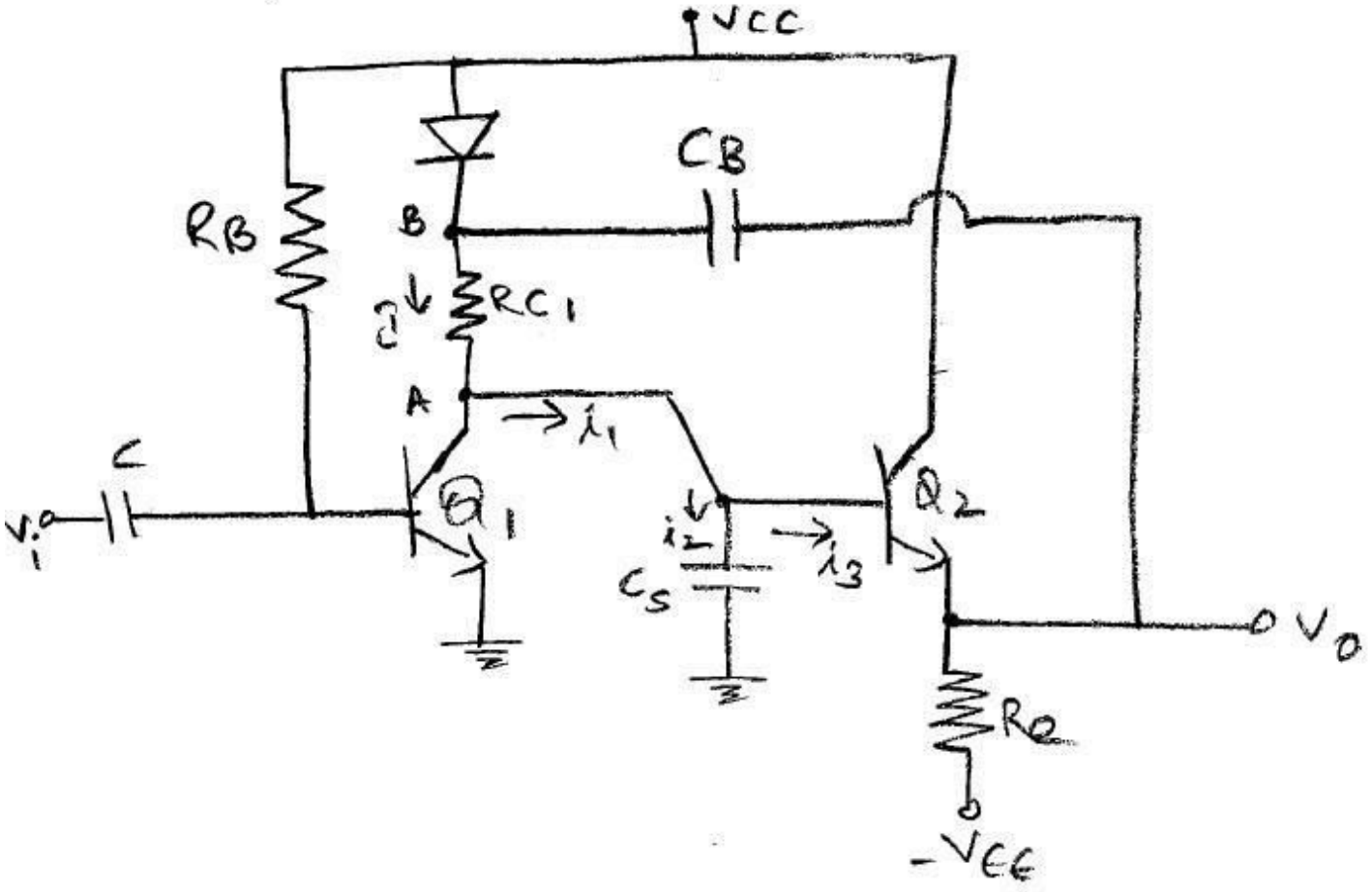


Input and output waveforms

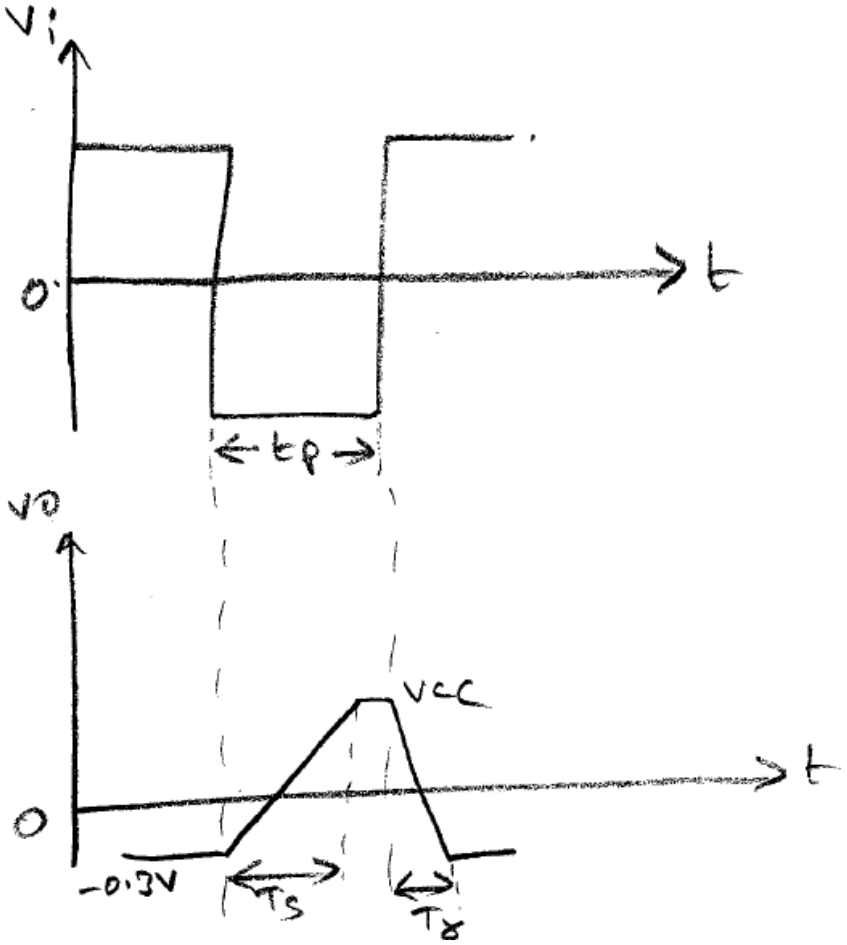


$T_S \leq T_P$

Transistor bootstrap time base generator



Input and output waveforms



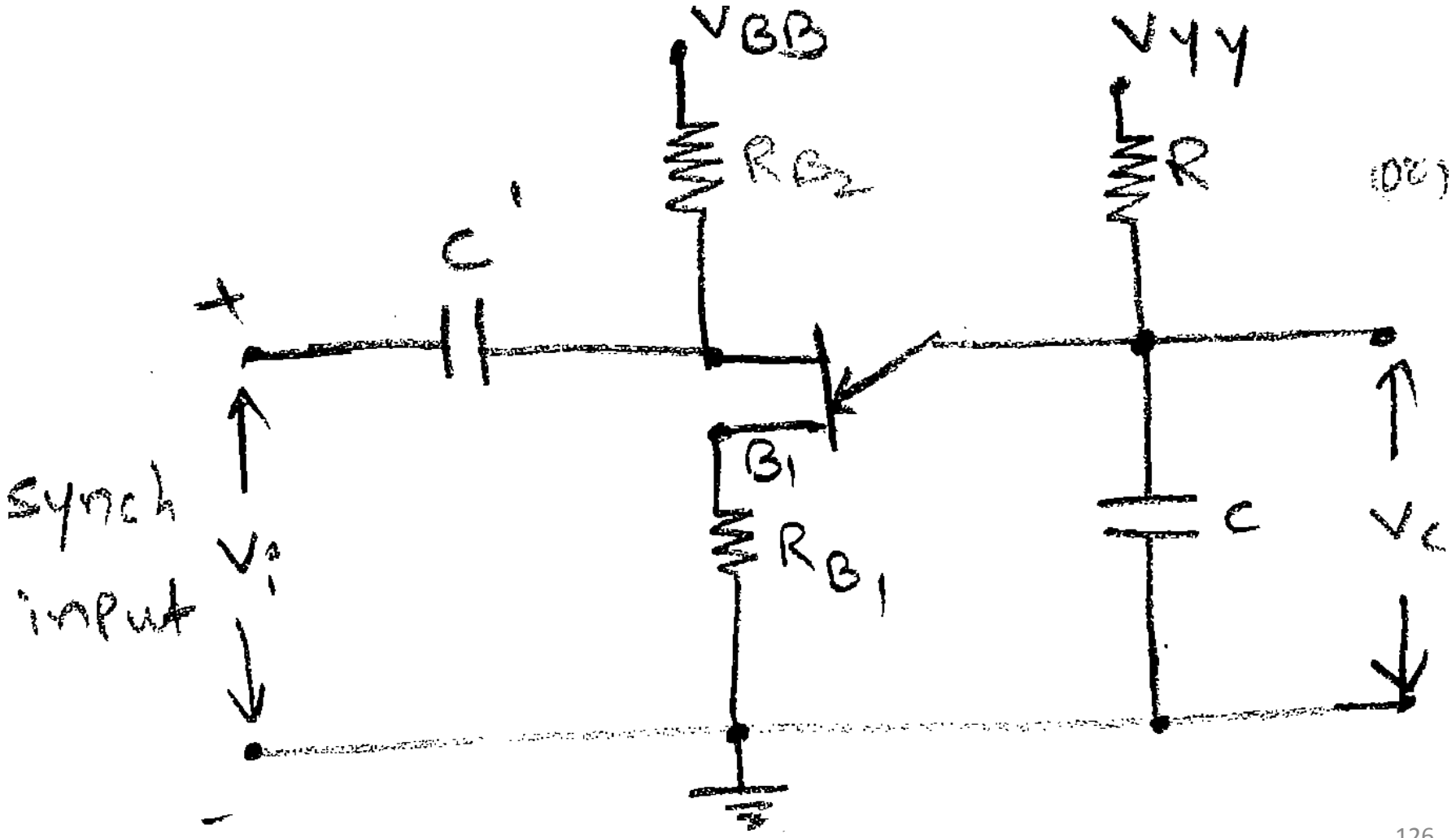
Comparision of Miller and Bootstrap time base generator

Bootstrap sweep circuit	Miller sweep circuit
1) The circuit employs positive feedback.	1) The circuit employs negative feedback.
2) The circuit generates positive going ramp.	2) The circuit generates negative going ramp.
3) The circuit employs an emitter follower whose gain is nearly unity.	3) The circuit requires an amplifier whose gain is very very large (ideally infinite).
4) The amplifier must have high input resistance.	4) Amplifier with high input resistance is not very essential.

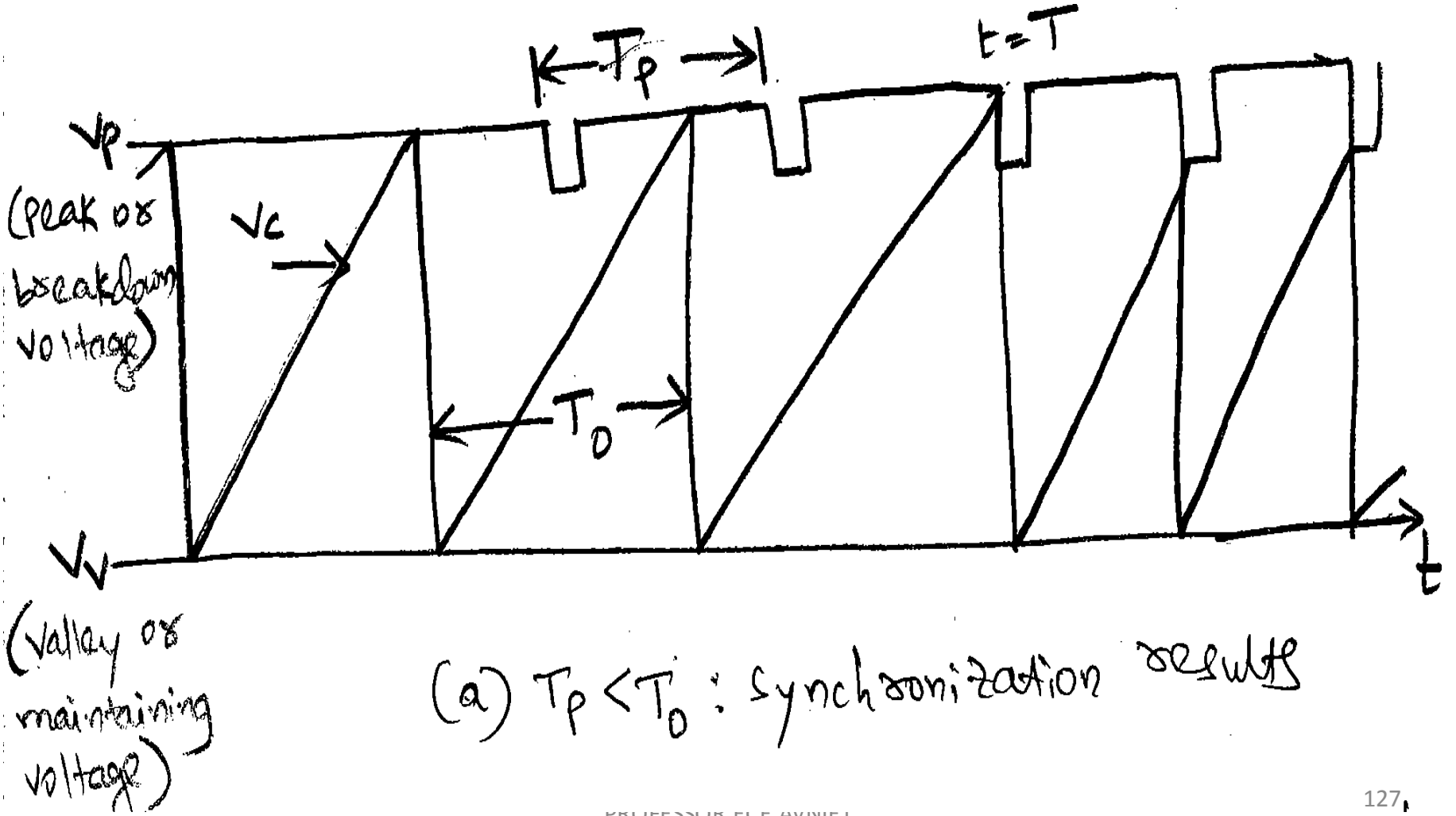
UNIT-5

SYNCHRONIZATION AND FREQUENCY DIVISION & LOGIC GATES

PULDE SYNCHRONIZATION OF RELAXATION DEVICES

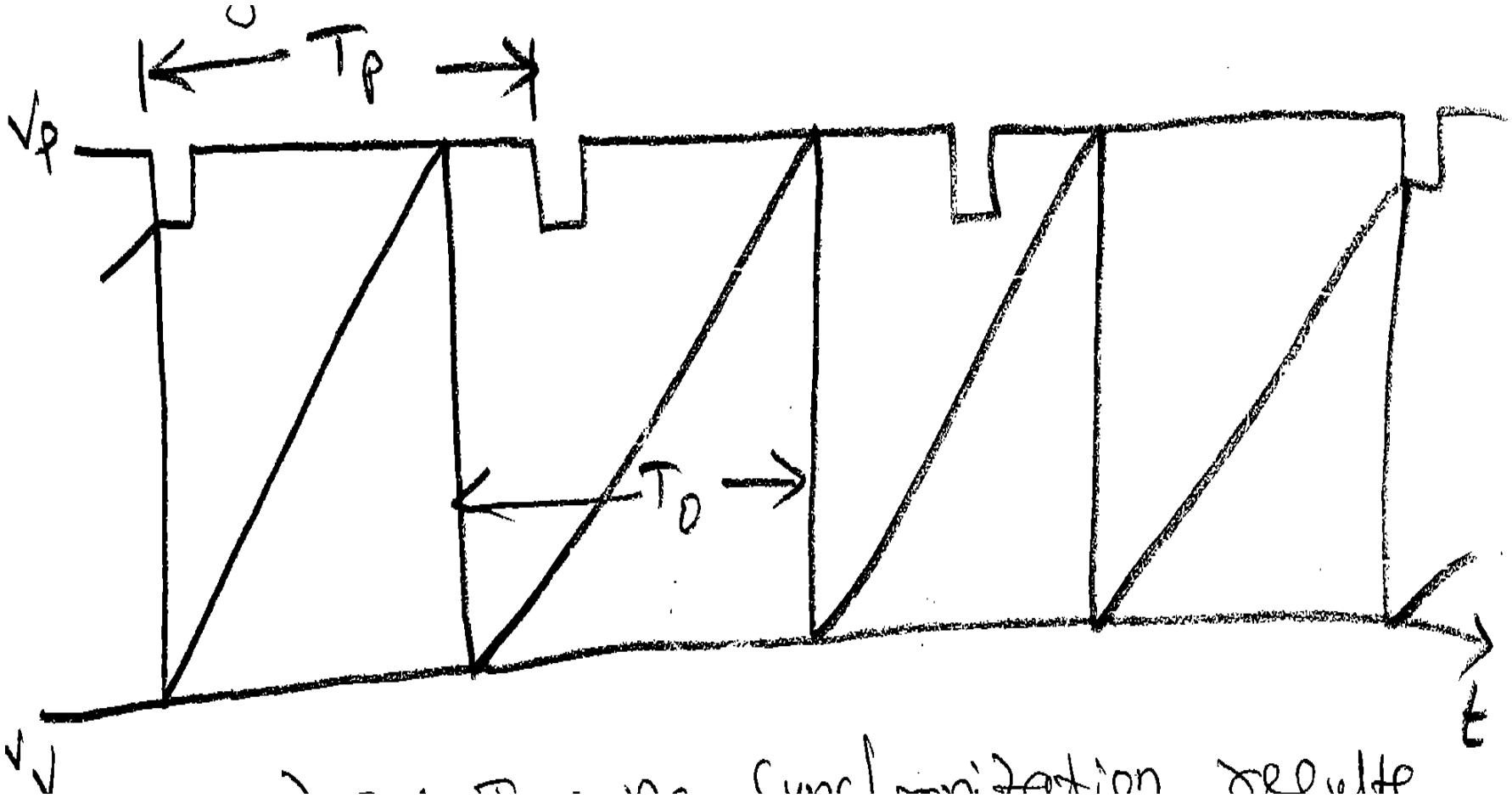


SHOWS THE SITUATION WHEN SYNCHRONIZATION PULSES ARE APPLIED

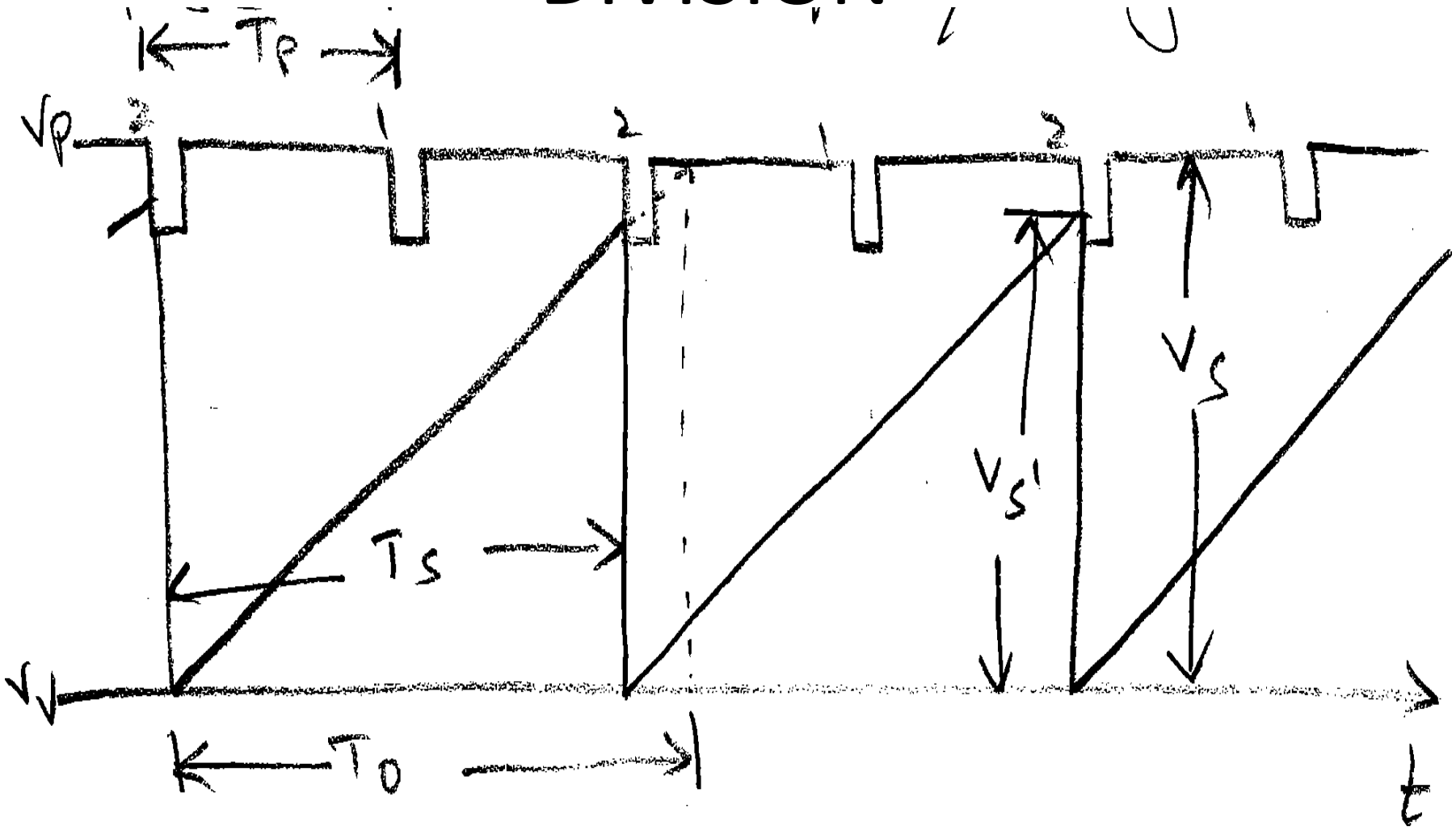


(a) $T_p < T_0$: Synchronization results

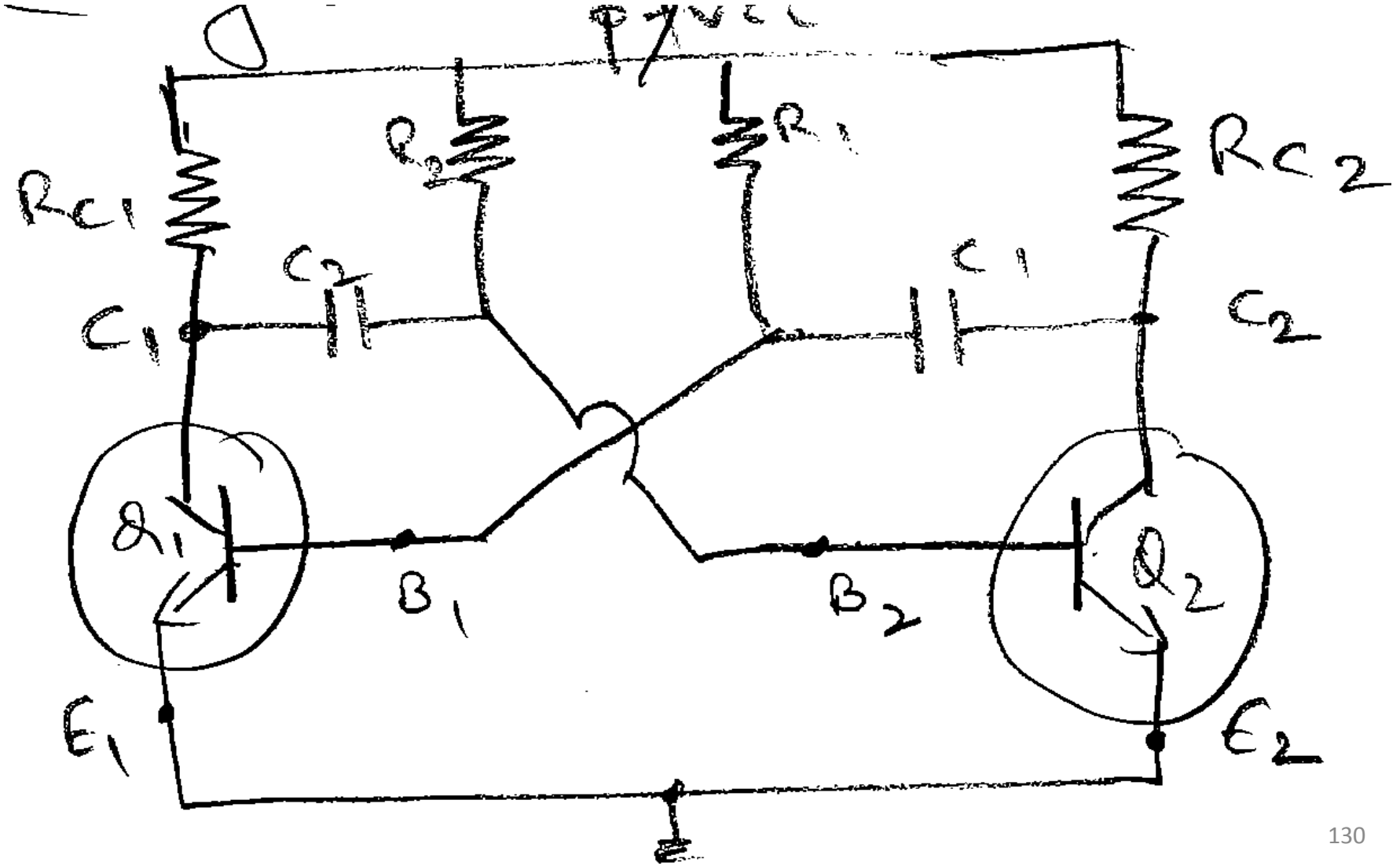
SHOWS THE CASE WHEN TP>TO



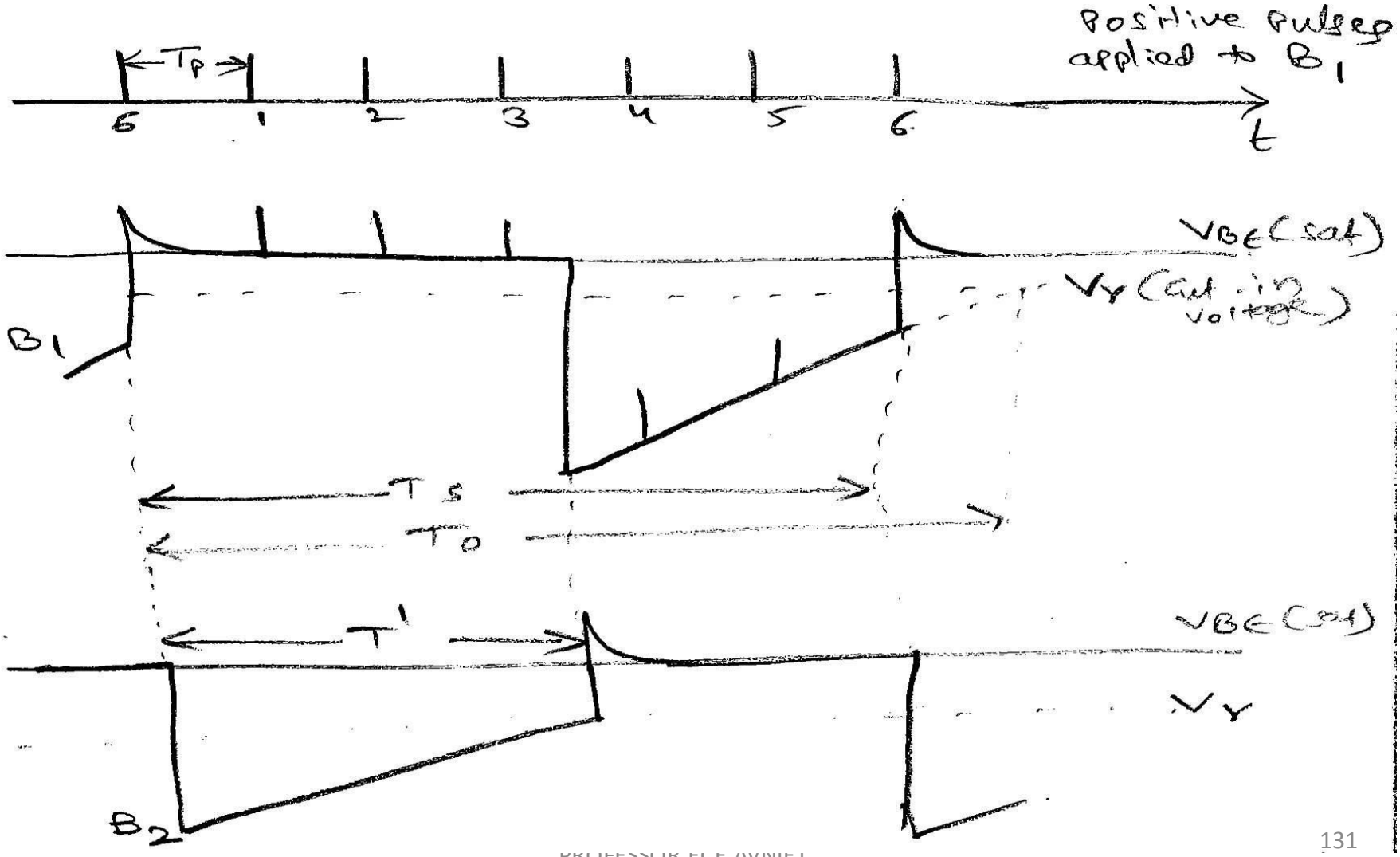
FREQUENCY DIVISION



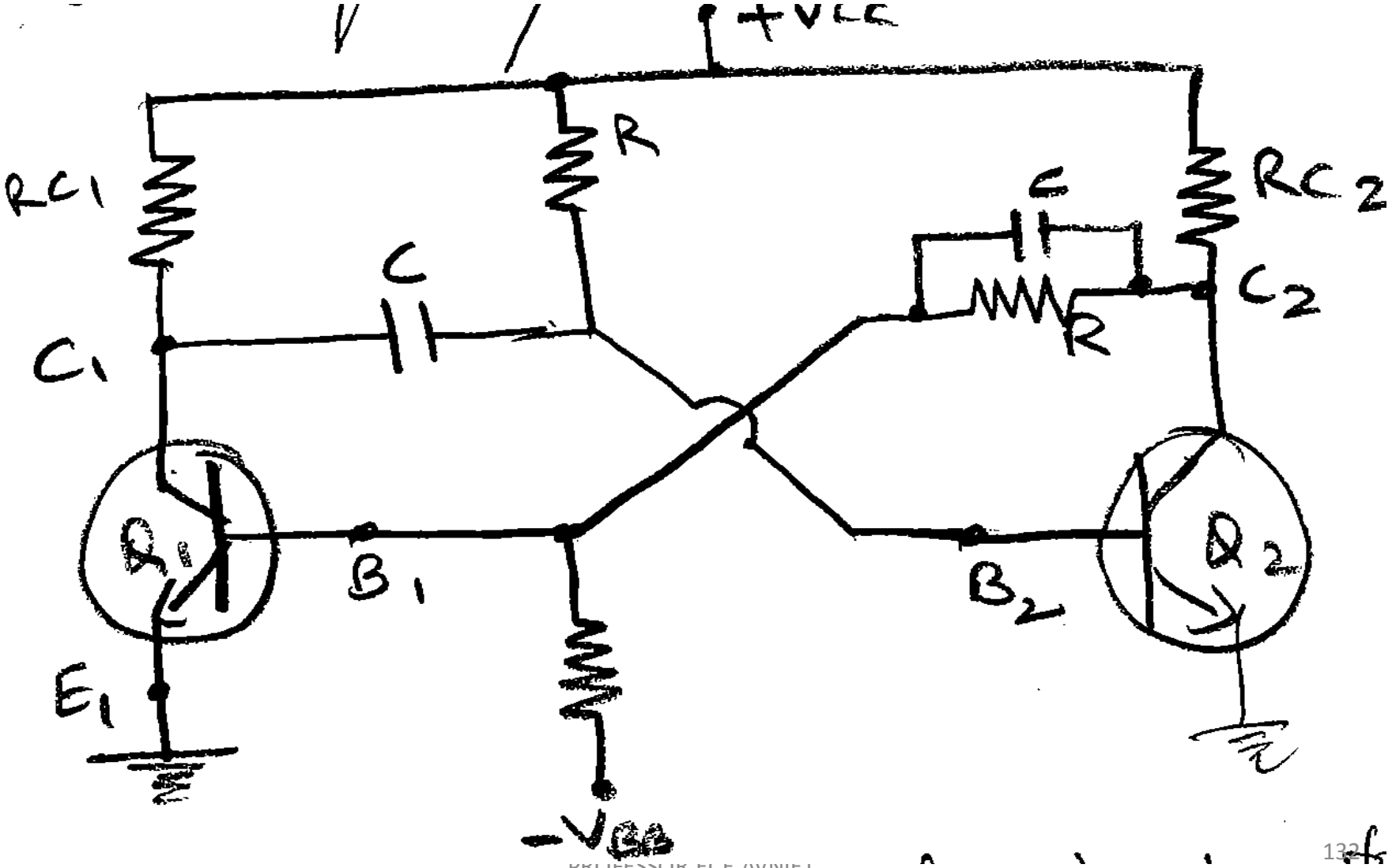
ASTABLE RELAXATION CIRCUIT



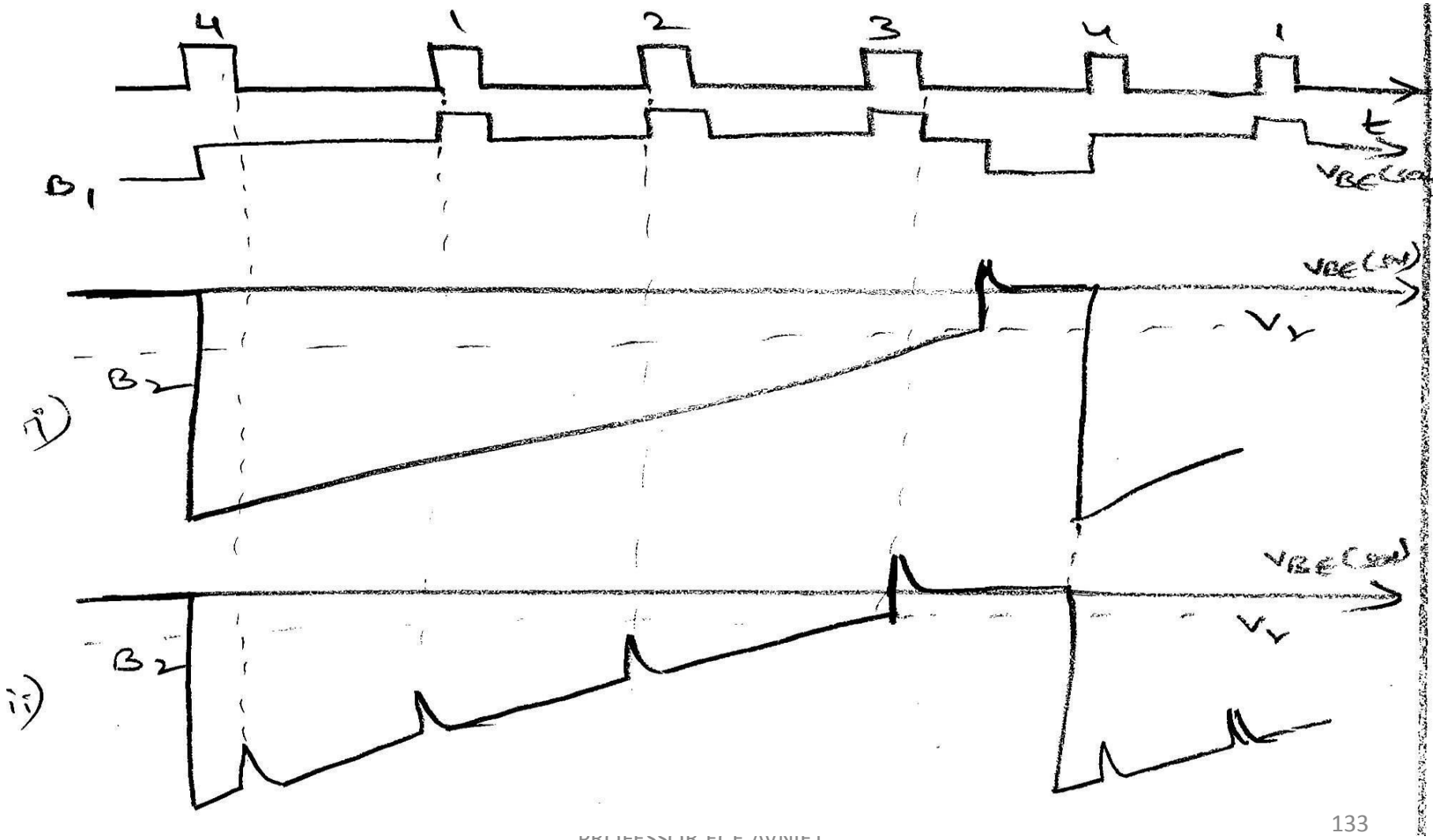
WAVEFORMS WHEN POSITIVE PULSES ARE APPLIED TOB1



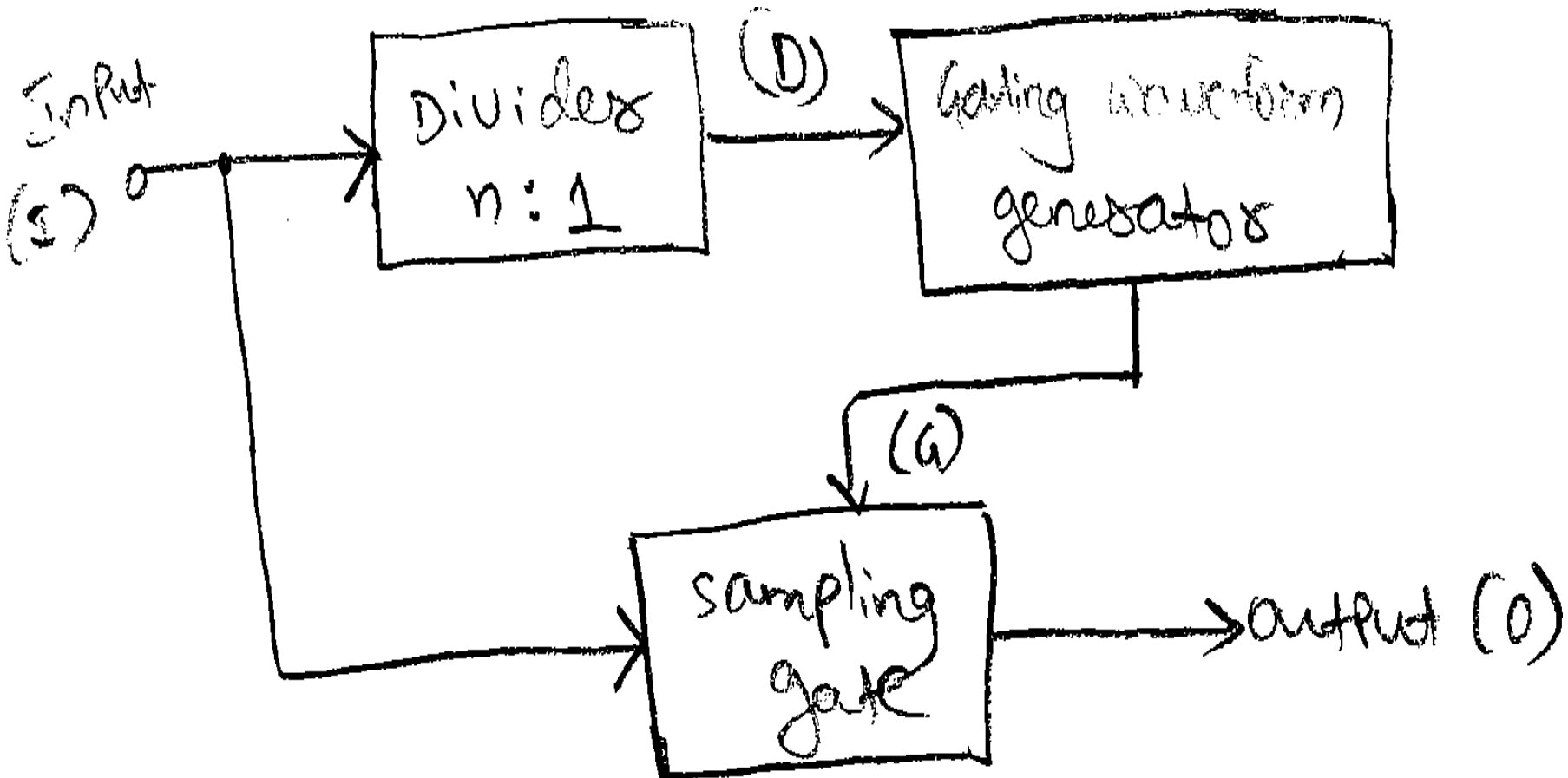
MONOSTABLE RELAXATION CIRCUIT



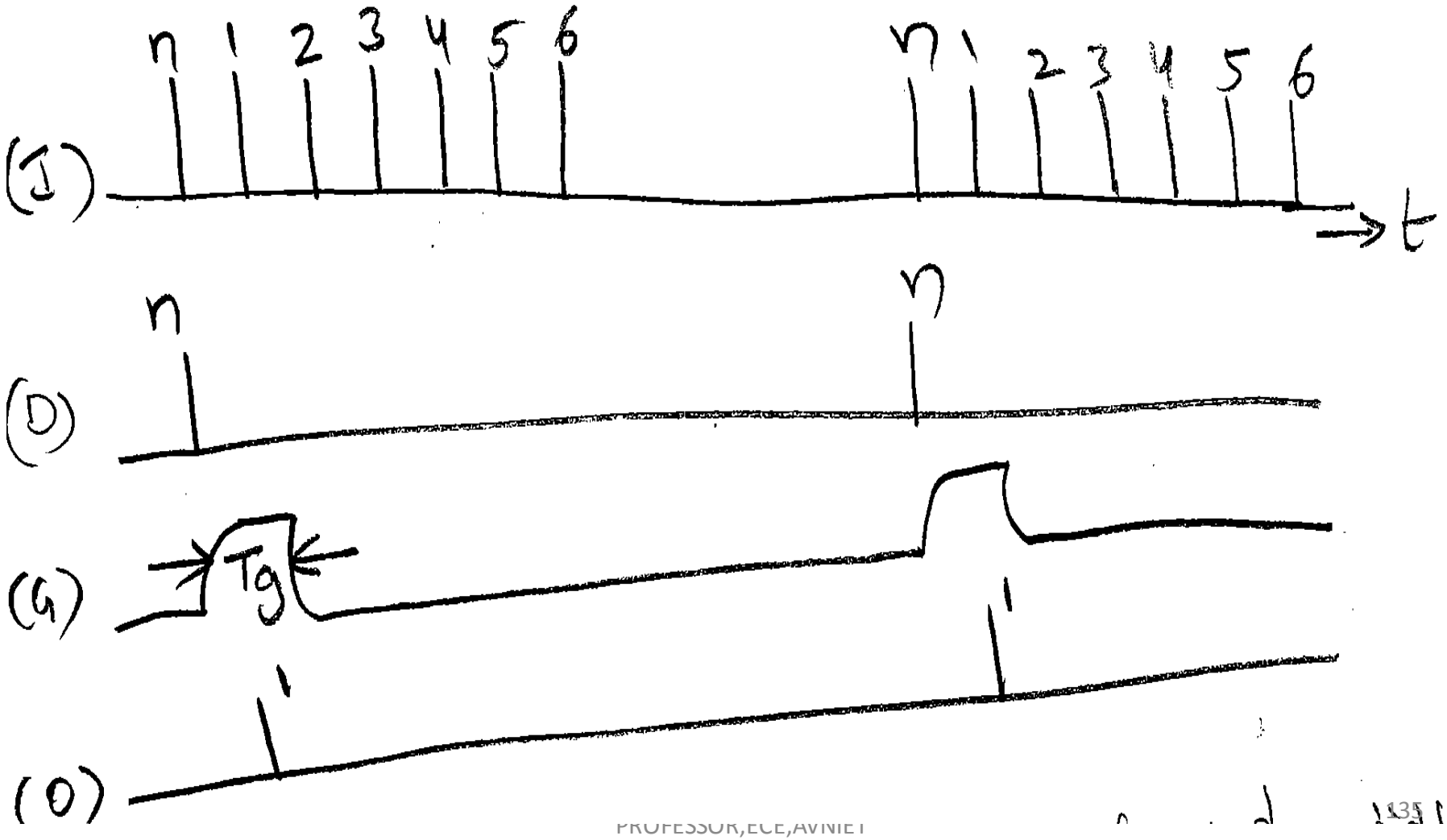
WAVEFORM AT B2 WITH NO PULSE OVERSHOOT AND WITH PULSE OVERSHOOT



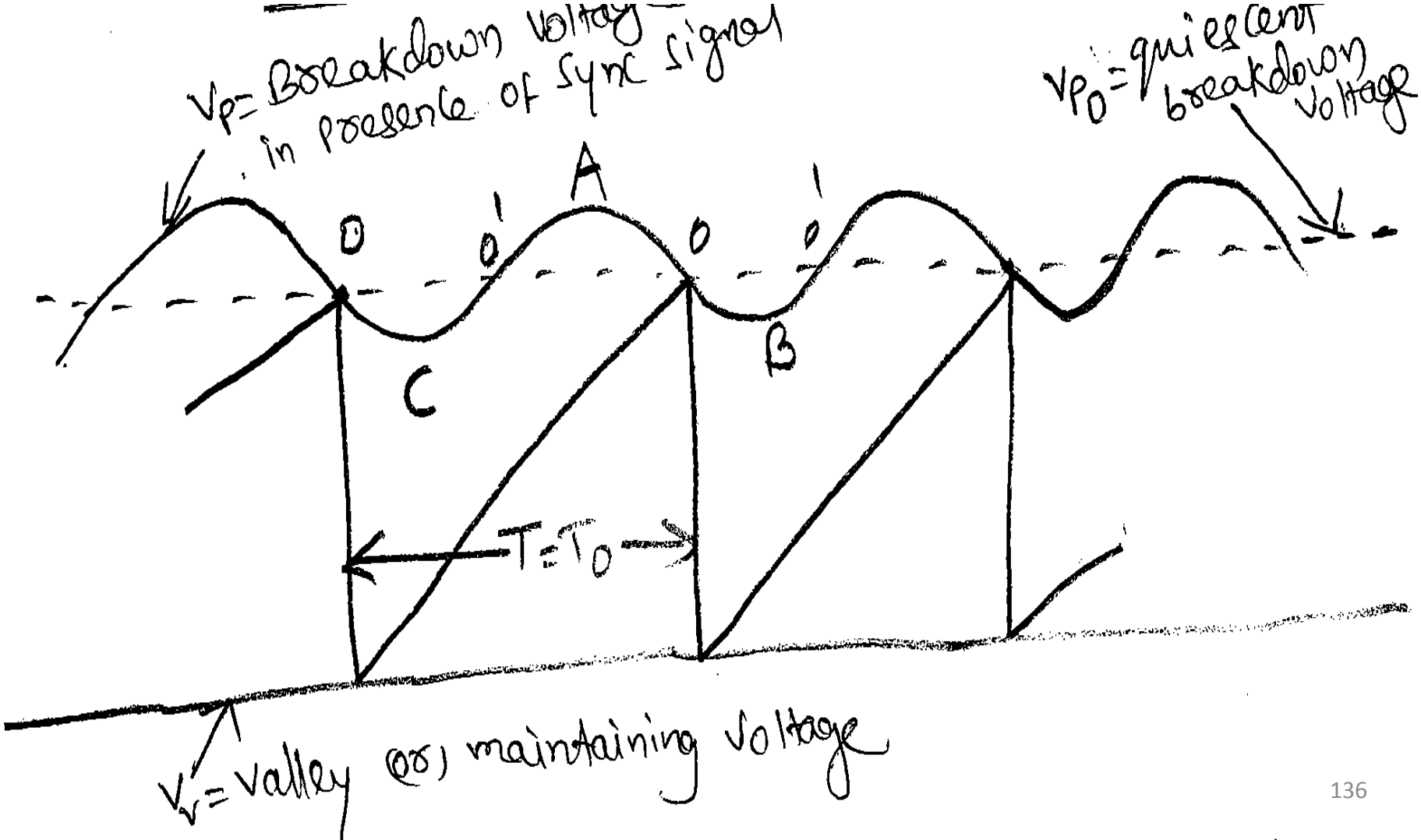
METHOD FOR ACHIEVING DIVISION WITH PHASE JITTER



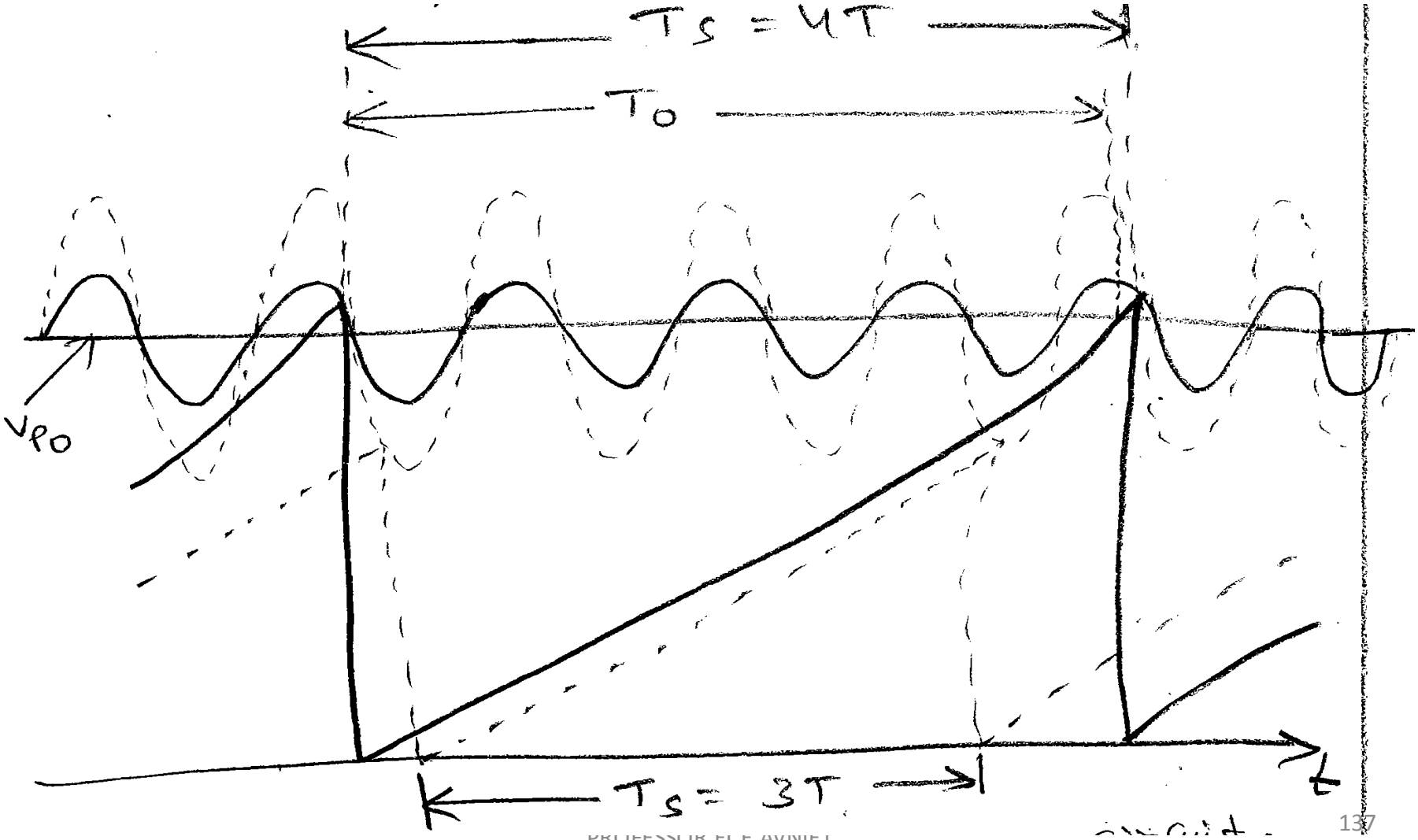
WAVEFORMS WITHOUT PHASE JITTER



SYNCHRONIZATION WITH SINE WAVE

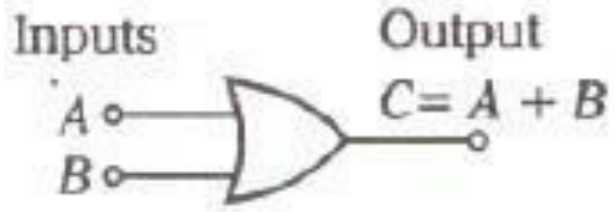


FREQUENCY DIVISION WITH SYNC SIGNAL



REALIZATION OF LOGIC GATES USING DIODES AND TRANSISTORS

- OR GATE
- OR GATE PERFORMS LOGICALADDITION.
- THE OR OPERATOR IS INDICATED BY APLUS (+) SIGN.

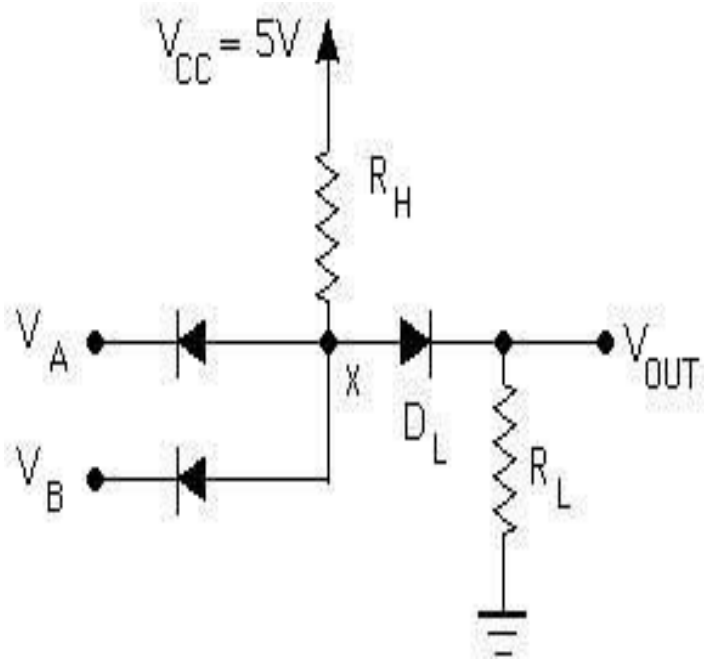


A	B	C = A + B
0	0	0
0	1	1
1	0	1
1	1	1

OR GATE USING DIODES

OPERATION:

- **ASSUME THE INPUT VOLTAGES ARE EITHER 0V (LOW) OR 5V (HIGH).**



BOTH AAND B ARE LOW:

- **THE DIODES ARE OFF AND WE CAN REPLACE THE**

Cont d.

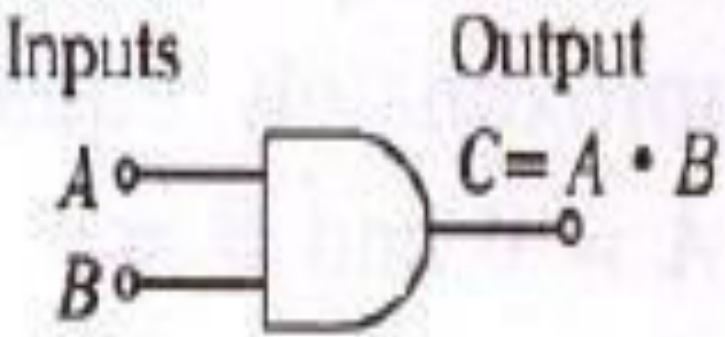
A IS LOW AND B IS HIGH:

- WHEN A IS LOW THE CORRESPONDING DIODE WILL BE OFF AND, B IS HIGH SO THE DIODE CORRESPONDS TO THE INPUT B WILL BE ON.
- NOW WE CAN REPLACE THE ON DIODE BY THE SHORT CIRCUIT EQUIVALENT AND THE OUTPUT C=5V.

- **B IS LOW AND A IS HIGH:**
  - WHEN B IS LOW THE CORRESPONDING DIODE WILL BE OFF AND, A IS HIGH SO THE DIODE CORRESPONDS TO THE INPUT A WILL BE ON.
  - NOW WE CAN REPLACE THE ON DIODE BY THE SHORT CIRCUIT EQUIVALENT AND THE OUTPUT C=5V.
- **BOTH A AND B ARE HIGH:**
  - WHEN BOTH THE INPUTS ARE HIGH BOTH THE DIODES WILL BE ON AND THE OUTPUT C=5V.

AND Gate

- THE AND GATE PERFORMS LOGICAL MULTIPLICATION.
- THE AND OPERATOR IS INDICATED BY USING ADOT (.) SIGN OR BY NOT SHOWING ANY OPERATOR SYMBOL ATALL.



A	B	C = A • B
0	0	0
0	1	0
1	0	0
1	1	1

AND GATE USING DIODES

- ASSUME THE INPUT VOLTAGES ARE EITHER 0V (LOW) OR 5V (HIGH).

BOTHAAND B ARE LOW:

- WHEN BOTH AAND B ARE LOW BOTH THE DIODES ARE ON AND WE CAN REPLACE THE DIODES BY SHORT CIRCUIT EQUIVALENT.
- HENCE POINT X IS CONNECTED TO GROUND AND OUTPUT C = 0V.
- **A IS LOWAND B IS HIGH:**

- WHEN A IS LOW THE CORRESPONDING DIODE WILL BE ON AND, B IS HIGH SO THE DIODE CORRESPONDS TO THE INPUT B WILL BE OFF.

- NOW WE CAN REPLACE THE ON DIODE BY THE SHORT CIRCUIT EQUIVALENT; HENCE POINT X IS CONNECTED TO GROUND AND THE OUTPUTC=0V.

Cont d.

B IS LOW AND A IS HIGH:

- WHEN B IS LOW THE CORRESPONDING DIODE WILL BE ON AND, A IS HIGH SO THE DIODE CORRESPONDS TO THE INPUT A WILL BE OFF.

- NOW WE CAN REPLACE THE ON DIODE BY THE SHORT CIRCUIT EQUIVALENT; HENCE POINT X IS CONNECTED TO GROUND AND THE OUTPUT C=0V.

BOTH A AND B ARE HIGH:

- BOTH THE DIODES WILL BE OFF AND THE OUTPUT C=5V.

NOT GATE (INVERTER)

- THE OUTPUT OF A NOT GATE IS THE COMPLEMENT OF THE INPUT.
- THE BUBBLE REPRESENTS INVERSION OR COMPLEMENT.

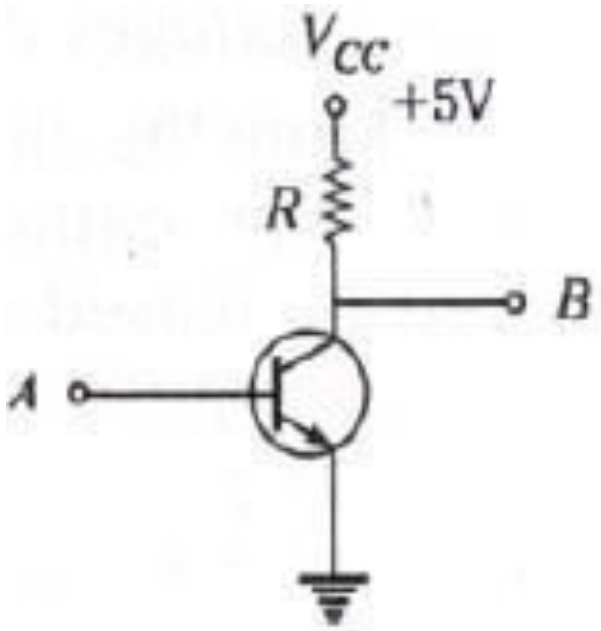
A	B
0	1
1	0

REALIZATION OF NOT GATE USING TRANSISTOR

A IS HIGH:

- When +5v is applied to a, the transistor will be fully on.
- So maximum collector current will flow and vcc =icr, making vc or voltage at point b as zero. [Recall ce loop kvl: vc=vcc-icr].
- **A IS LOW:**

When 0v is applied to a, the transistor will be cut-off.
So ic=0ma and vc or voltage at point b is equal to vcc.



Logic Families

Logic Families Vocabulary

Vocabulary

TTL (Transistor Transistor Logic) Integrated-circuit technology thatuses the bipolar transistor as the principal circuit element.

CMOS (Complimentary Metal Oxide Semiconductor) Integrated-circuit technology that uses the field-effect transistor as the principal circuit element.

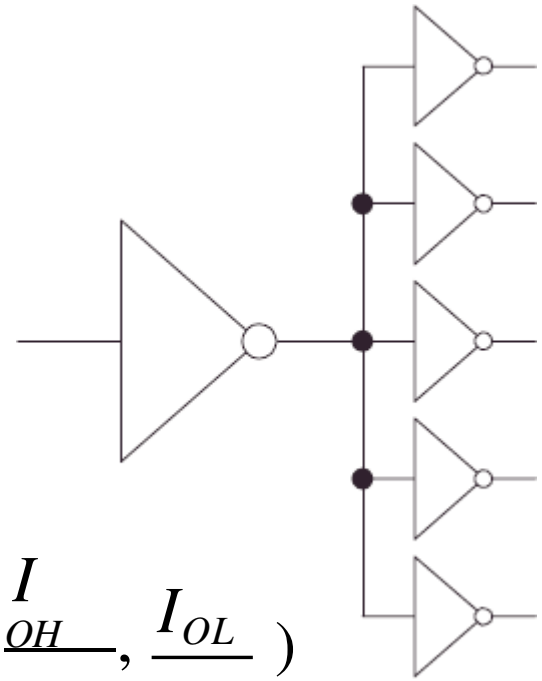
ECL (Emitter Coupled Logic) Integrated-circuit technology that uses the bipolar transistors configured as a differential amplifier. This eliminates saturation and improves speed but uses more power than other families.

OTHER DIGITAL IC SPECIFICATIONS

- Drive Capabilities- sometimes referred to as fan-in or fan-out.
- Fan out- number of inputs of a logic family that can be driven by a single output. The drive capability of outputs.
- Fan in- the load an input places on an output.
- Propagation delay- has to do with the "speed" of the logic element. Lower propagation delays mean higher speed which is a desirable characteristic.
- Power Dissipation- generally, as propagation delays *decrease*, power consumption and heat generation *increase*. CMOS is noted for low power consumption.

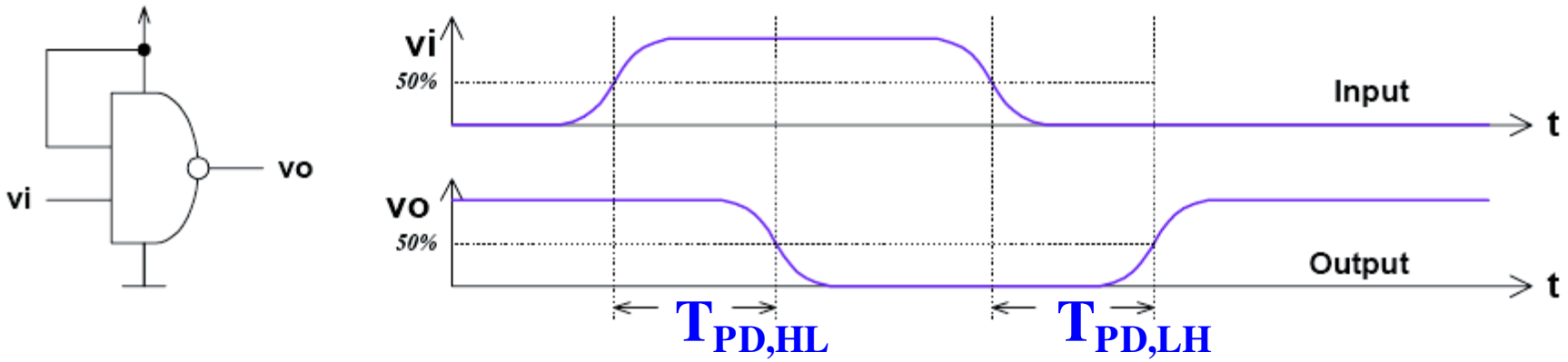
Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably



DC fanout $= \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$

Logic families: propagation delay

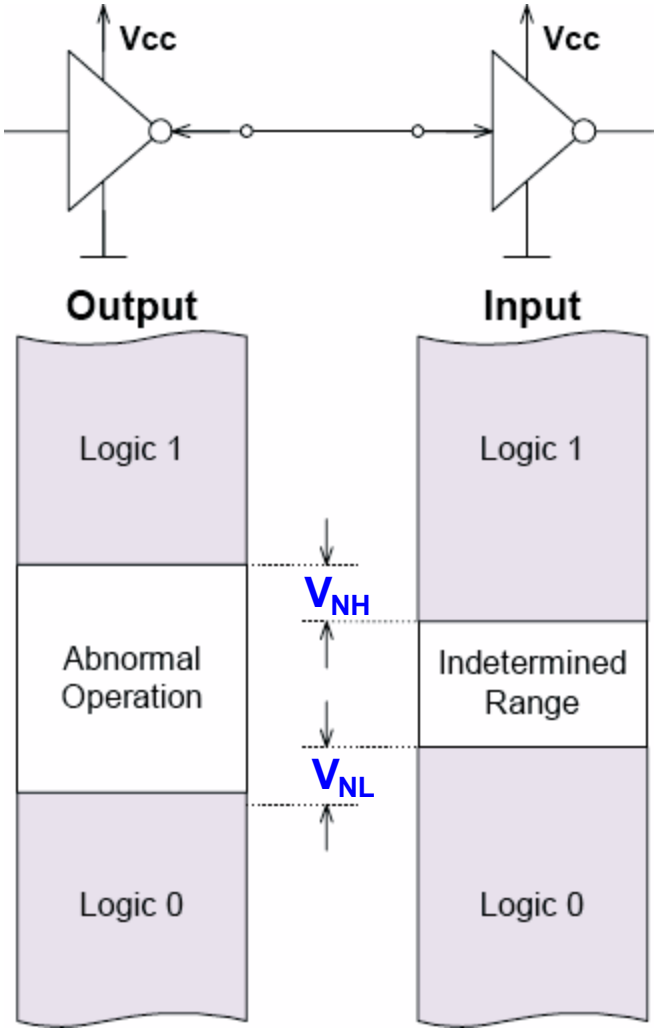


$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$

Logic families: noise margin



HI state noise margin:

$$V_{NH} = V_{OH}(\min) - V_{IH}(\min)$$

LO state noise margin:

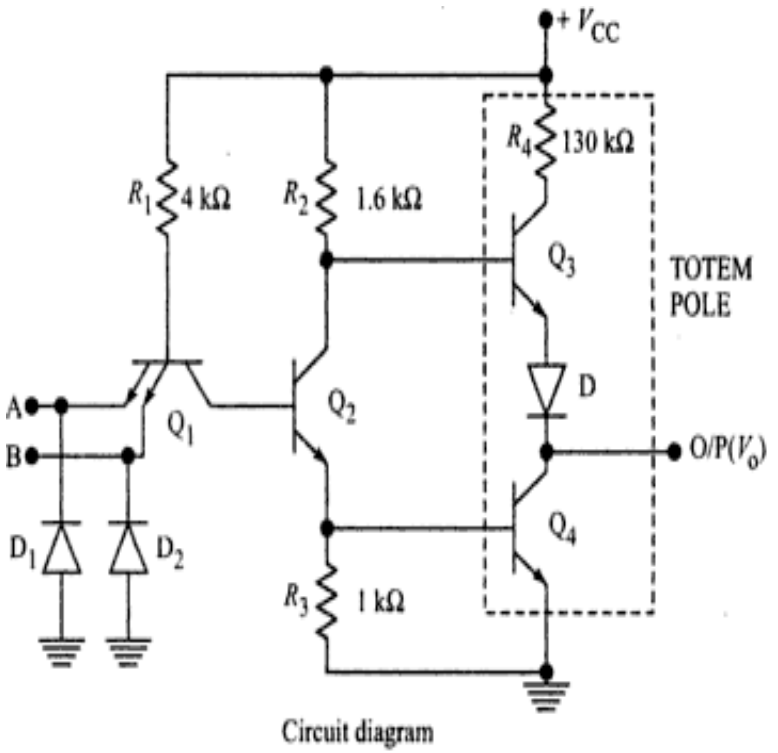
$$V_{NL} = V_{IL}(\max) - V_{OL}(\max)$$

Noise margin:

$$V_N = \min(V_{NH}, V_{NL})$$

TOTEM POLE NAND GATE

- First introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

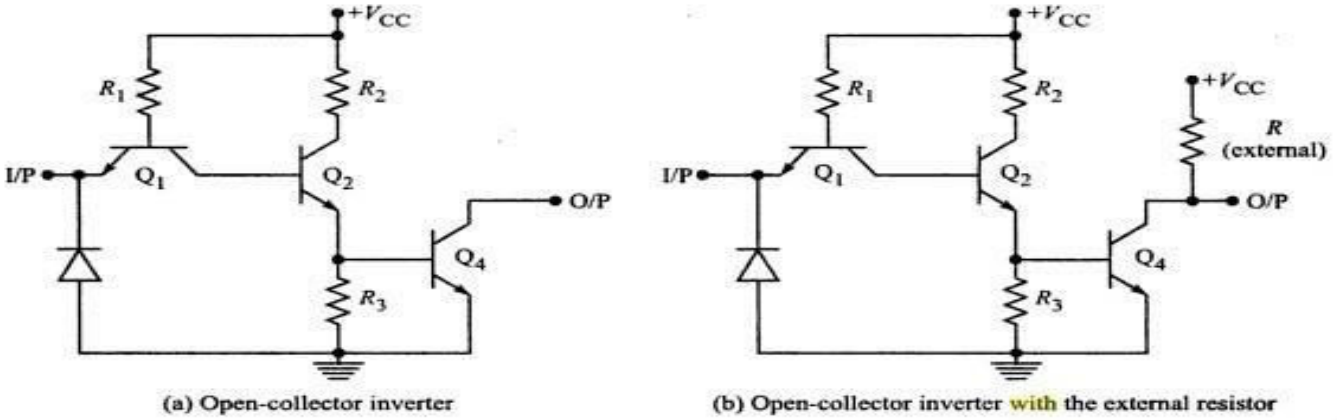


Circuit diagram

Figure 9.1 TTL NAND gate.

Open collector gate

- An **open collector** is a common type of output found on many integrated circuits (IC).
- Instead of outputting a signal of a specific voltage or current, the output signal is applied to the base of an internal NPN transistor whose collector is externalized (open) on a pin of the IC. The emitter of the transistor is connected internally to the ground pin. If the output device is a MOSFET the output is called **open drain** and it functions in a similar way



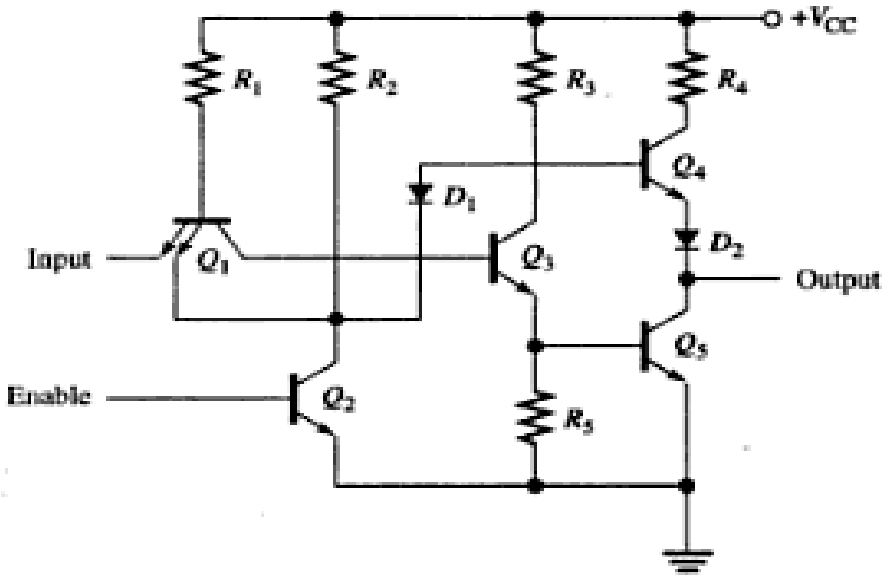
(a) Open-collector inverter

(b) Open-collector inverter with the external resistor

Figure 9.2 Circuit diagram of open-collector inverter.

Tristate TTL

- Tristate means a state of logic other than „1“ and „0“ in which there is a high impedance state and there is no isource or isink at the output stage transistor (or MOSFET). A gate capable of being in „1“, „0“ and tristate is know



Direct-coupled transistor logic (DCTL)

- than RTL gates. Unfortunately, DCTL has much smaller signal levels, has more susceptibility to ground noise, and requires matched transistor characteristics. The transistors are also heavily
- overdriven; that is a good feature in that it reduces the saturation
- voltage of the output transistors, but it also slows the circuit down
- due to a high stored charge in the base.[1] Gate fan-out is limited due to current hogging: if the transistor base-emitter voltage (V_{BE}) are not well matched, then the base-emitter junction of one transistor may conduct most of the input drive current at such a low base-emitter voltage that other input transistors fail to turn on

Direct-coupled transistor logic (**DCTL**) is similar to resistor–transistor logic (RTL) but the input transistor bases are connected directly to the collector outputs without any base resistors. Consequently, DCTL gates have fewer components, are more economical, and are simpler to fabricate onto integrated circuits

ECL

Emitter-Coupled Logic (ECL)

- PROS: Fastest logic family available (~1ns)
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. "0": –1.7V. "1": –0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
- Open LTspice example: ECL inverter…

ECL
EMITTER COUPLED LOGIC

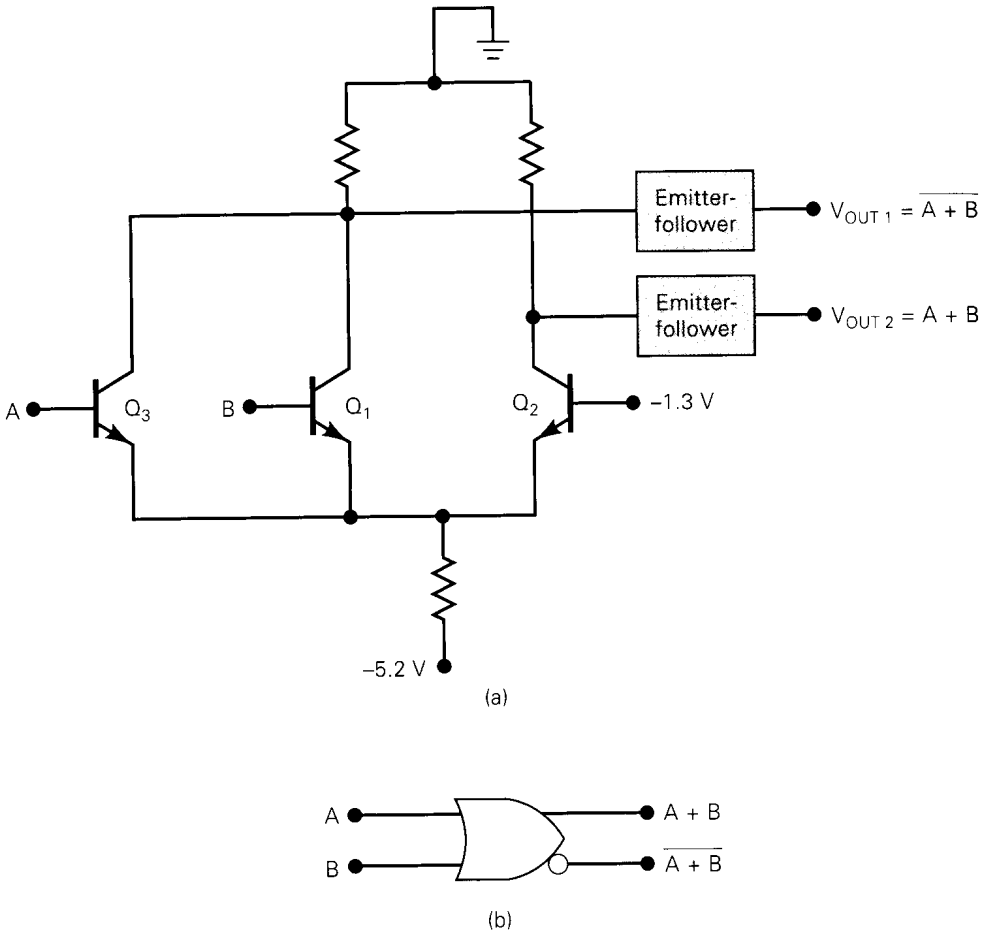


Figure 8-30 (a) ECL NOR/OR circuit; (b) logic symbol.

LOGIC FAMILIES AND INTRODUCTION

- WE HVE SEEN THAT DIFFERENT DEVICES USE DIFFERENT VOLTAGES RANGES FOR THEIR LOGIC LEVELS.
- THEY ALSO DIFFER IN OTHER CHARACTERISTICE
- IN ORDER TO ASSURE CORRECT OPERATION WHEN GATES ARE INTERCONNECTED THEY ARE NORMALLY PRODUCED IN LOGIC FAMILIES
- THE MOSTLY WIDELY USED FAMILIES ARE
  - COMPLEMENTARY METAL OXIDE (CMOS)
  - TRANSISTOR- TRANSISTOR LOGIC (TTL)
  - EMITTER COUPLED LOGIG (ECL)

COPARISON OF LOGIC FAMILIES

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Very good	Good
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4