A

Laboratory Manual

For

LICA LAB

(B. Tech Electronics and Communication Engineering)

YEAR-III B. tech ECE SEM-I

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PROGRAMOUTCOMES(POs)

PO Name	Graduate Attributes	PO Statements
PO1	Engineering knowledge	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	Problem analysis	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	Design/ development of solutions	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	Modern tool usage	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	The engineer and society	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO 9	Individual and team work	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

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PO 10	**Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance**	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning**	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSOs Name	Program Specific Outcome Statements
PSO - 1	An ability to apply the concepts of Electronics, Communications, Signal Processing, VLSI, Control Systems etc, in the design and implementation of application oriented engineering systems.
PSO – 2	An ability to solve complex Electronics and communication engineering problems, using latest hardware and software tools, along with analytical and managerial skills to arrive appropriate solutions, either independently or in team.

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AVN INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

VISION – MISSION – PEOs

Institute Vision	"To be a Centre of excellence in technical education and to become an Epic Centre of Research for Creative solutions"
Institute Mission	"To address the Emerging needs through Quality technical Education with an Emphasis on Practical Skills and advanced Research with Social Relevance"
Department Vision	To become a Centre of excellence in the field of Electronics and Communication Engineering, keeping in view of advanced developments that produces Innovative, Skillful, Socially responsible professionals who can contribute significantly to Industry and Research.
Department Mission	1).To provide the skilled manpower with state-of-art knowledge in Electronics and Communication Engineering 2).To provide the Professionals to the nation with innovations and ideas in the area of advanced Electronics and Communication Technologies through research and graduate studies. 3).To provide the professionals for participating in the design and development process of industries and society.
Program Educational Objectives(PEOs)	**PEO 1:** Graduates will be able to synthesize mathematics, science, engineering fundamentals; laboratory and work-based experience to formulate and solve problems related to the Electronics and Communication Engineering and shall develop proficiency in computer-based engineering and the use of computational tools. **PEO 2:** Graduates will be prepared to communicate and work team-based on the multi-disciplinary projects practicing the ethics of their profession with a great sense of social responsibility. **PEO 3:** Graduates will recognize the importance of lifelong learning to shine as experts either as entrepreneurs or as employees and thereby broadening their professional knowledge.

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COURSE OBJECTIVES

S. No	Course Objectives
EC505PC.1	Analyze and design various Linear applications using Op-amp.
EC505PC.2	Design and construct waveform generation circuits
EC505PC.3	To design the non-linear application of op-amp such as Schmitt circuit.
EC505PC.4	Analyze the application of 555 timer and 565 PLL ICs.
EC505PC.5	Analyze the functionality of various voltage regulator ICs such as IC 7805, IC-IC-7809 etc

COURSE OUTCOMES

At the end of the Course/Subject, the students will be able to:

S. No	Course Outcomes(COs)	BTL
EC505PC.1	Design and analyze the basic op-amp application such as Inverting amplifier, non-inverting amplifier, adder, subtractor, and comparator Circuits using OP-AMP IC-741	Create
EC505PC.2	Verify the functionality of op-amp application such Integrator, Differentiator and Schmitt Trigger Circuits using OP-AMP IC-741	Evaluate
EC505PC.3	Analyze the performance of op-amp application LPF, HPF, Waveform generatorsusing OP-AMP IC-741	Analysis
EC505PC.4	Verify the functionality of IC-555 based applications such Monostable andAstableMultivibrator Circuits and IC 565 – PLL Applications.	Evaluate
EC505PC.5	Analyze general purpose VoltageRegulator using IC-723 and Three Terminal Voltage Regulators using IC-7805, IC-7809, IC-7912.	Analysis

CONTENTS

Linear IC Experiments

1. Inverting and Non-inverting Amplifiers using Op Amps.
2. Adder and Subtractor using Op Amp.
3. Comparators using Op Amp.
4. Integrator Circuit using IC 741.
5. Differentiator circuit using Op Amp.
6. Active Filter Applications – LPF, HPF (first order)
7. IC 741 Waveform Generators – Sine, Square wave and Triangular waves.
8. Mono-stable Multi-vibrator using IC 555.
9. Astable Multi-vibrator using IC 555.
10. Schmitt trigger Circuits- using IC-741.
11. IC-565- PLL applications.
12. Voltage Regulator using IC 723.
13. Three Terminal Voltage Regulators –7805, 7809, 7912.

Additional Experiments

1. Averaging Amplifier
2. Zero Crossing Detector
3. Voltage Follower/Unity gain amplifier

EQUIPMENTS REQUIRED

1. CRO
2. 1 MHz Function Generator (sine, square, triangular).
3. Regulated Power Supply.
4. Multi-meter or Voltmeter.

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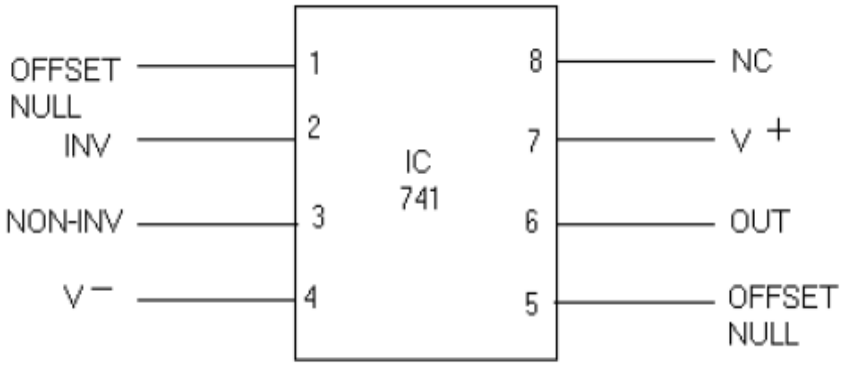
IC µA 741 OP-AMP



1. Supply voltage:

µA 741A, µA 741, µA 741E ---------- ±22V

µA 741C ---------- ±18 V

2. Internal power dissipation

DIP package ---------- 310 Mw.

3. Differential input voltage ---------- ±30 V.

4. Operating temperature range

Military (µA 741A, µA 741) -- ---------- -550 to +1250 C.

Commercial (µA 741E, µA 741C) ---------- 00 C to +700 C.

5. Input offset voltage ---------- 1.0 mV.

6. Input Bias current ---------- 80 nA.

7. PSSR ---------- 30 µV/V.

8. Input resistance ---------- 2MΩ.

9. CMMR ---------- 90.

10. Output resistance ---------- 75Ω.

11. Bandwidth ---------- 1.0 MHz.

12. Slew rate ---------- 0.5 V/µ sec.

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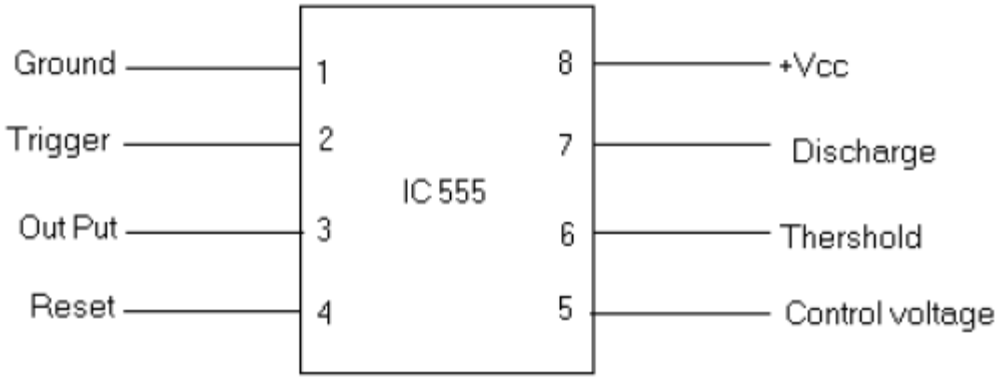
NE / SE 555 / SE 555C



1. Supply voltage ---------- 4.5 V to 18 V
2. Supply current ---------- 3mA
3. Output voltage (low) ---------- 0.1 V
4. Output voltage (high) -------- 12.5 V (15 V Vcc) & 3.3 V (5V Vcc)
5. Maximum operating frequency ---------- 500 KHz
6. Timing from μ sec to hours

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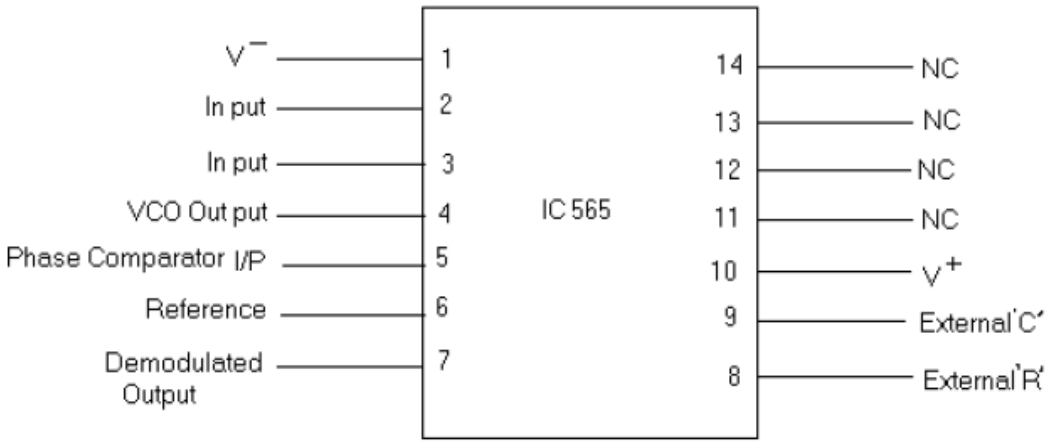
Phase Locked Loop NE / SE 565



1. Maximum supply voltage : 26 V
2. Input Voltage : 3 V(P-P)
3. Power dissipation : 300Mw
4. Operating temperature : NE 565- 00 C to 700C (SE 565-55 to +1250 C
5. Supply voltage : 12 V
6. Supply current : 8 mA
7. Output current- (sink) : 1 mA

(Source) : 10 mA

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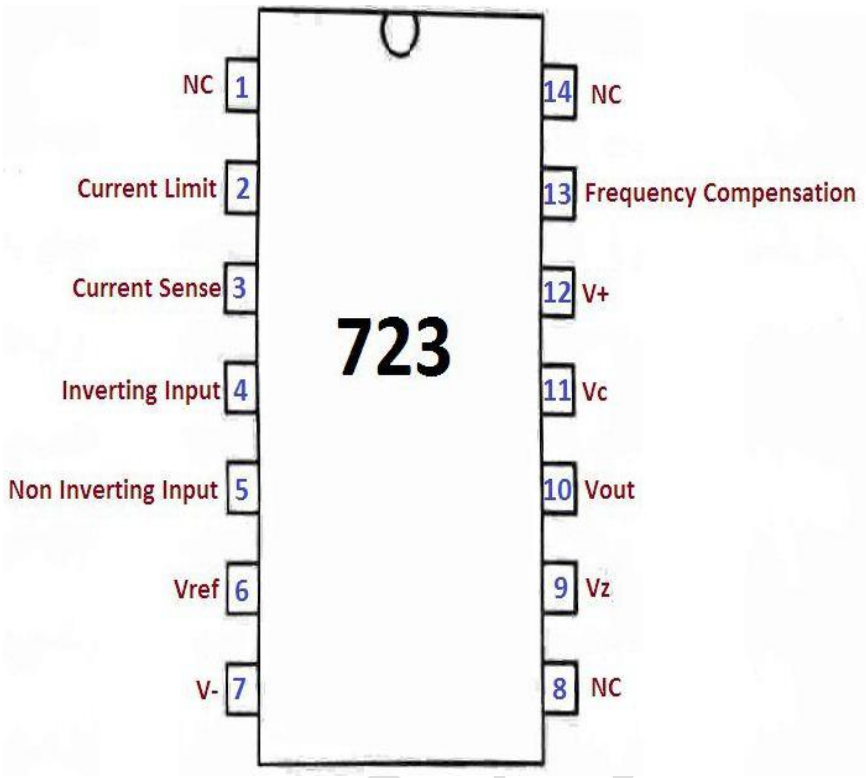
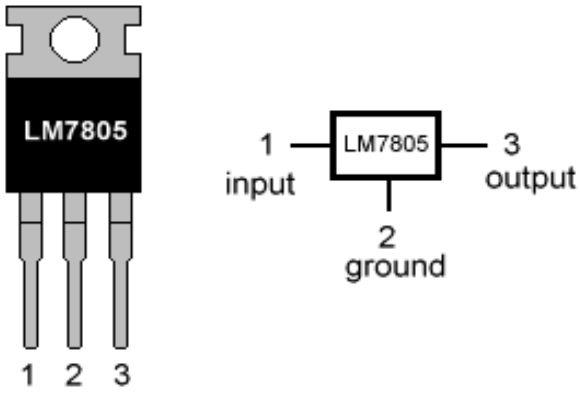


The important features of IC 723 regulators are as given below

1. It has small in size and lower in cost.
2. It operates in positive or negative supply operation.
3. It has choice of supply voltage.
4. Wide variety of applications such as series, shunt, switching and floating regulators.
5. Relative simplicity with power supply can be designed.
6. Low standby current gain.
7. Very low temperature drift and high ripple rejection.
8. Built in fold back current limiting.
9. Input voltage is maximum 40 V.
10. Output voltage adjustable from 2 V to 37 V.
11. Output current upto 150 mA without external pass transistor.

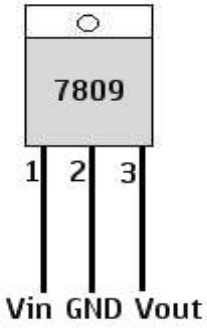
LM7805 PINOUT DIAGRAM



PIN 1-INPUT: The function of this pin is to give the input voltage. It should be in the range of 7V to 35V. We apply an unregulated voltage to this pin for regulation. For 7.2V input, the PIN achieves its maximum efficiency.

PIN 2-GROUND: We connect the ground to this pin. For output and input, this pin is equally neutral (0V).

PIN 3-OUTPUT: This pin is used to take the regulated output. It will be$5V(4.8V - 5.2V)$



Specifications:

1. Output Type: Fixed
2. Output Voltage: +9V dC
3. Current Output: up to 1.5A
4. Input Voltage: 11.5 - 35VDC
5. Quiescent (standby) current: 8mA
6. Dropout Voltage (Max): 2 V @ 1A
7. Category: Linear Voltage Regulators - Standard
8. Polarity: Positive
9. Operating Temperature: 0 to +125°C
10. Mounting Style: Through Hole
11. Pin Spacing Pitch: 2.54mm
12. Hole Diameter: 3.8mm
13. Dimensions: 10.4 x 4.6 x 9.15mm

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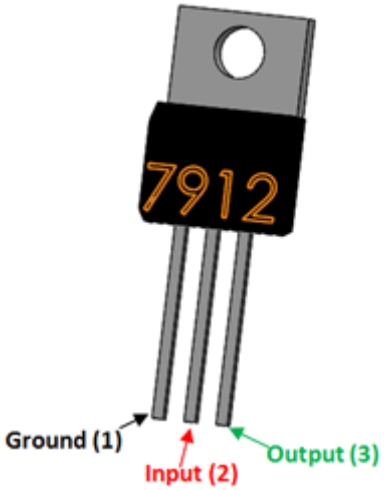

Pin Configuration

Pin Number	Pin Name	Description
1	Ground (Gnd)	Connected to Ground
2	Input (V+)	Unregulated Input Voltage
3	Output (Vo)	Outputs Regulated -12V

7912 Regulator Features

1. 12V Negative Voltage Regulator
2. Minimum Input Voltage is -14.5V
3. Maximum Input Voltage is -27V
4. Peak Output Current is 2.2A
5. Average Output Current is upto 1A
6. Internal Thermal Overload and Short circuit current limiting protection is available.
7. Available in TO-220 package only.

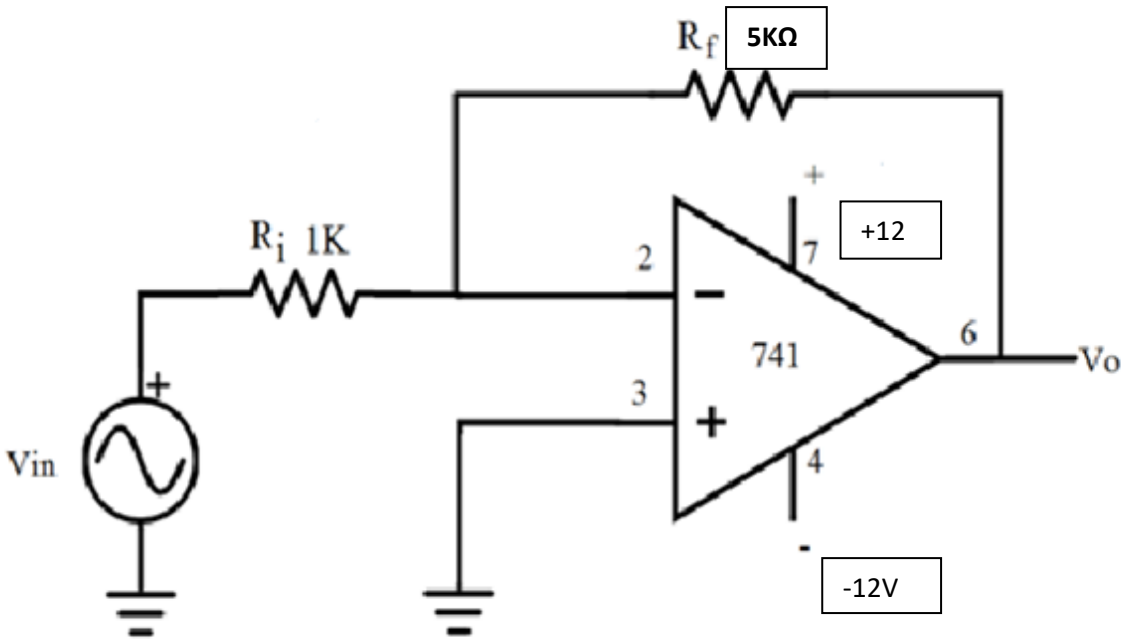

Fig 1.1 Inverting amplifier using op-amp.

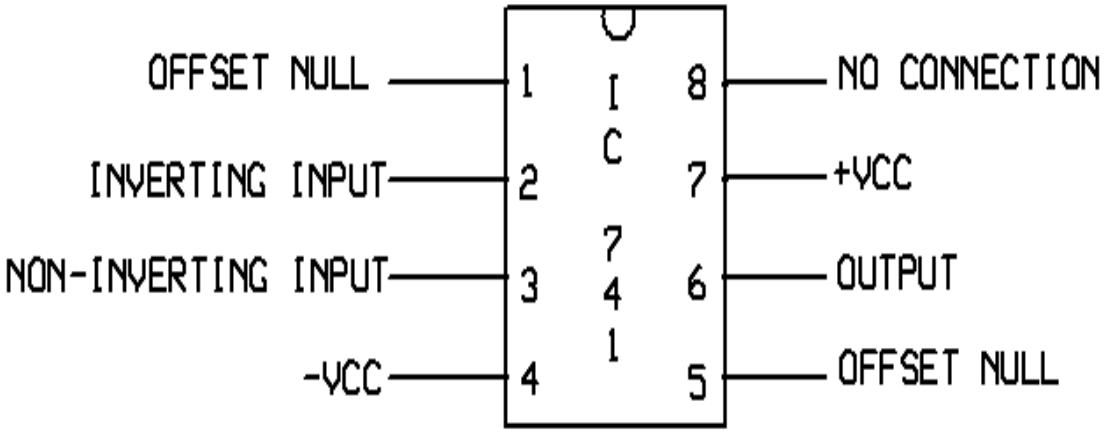

Fig 1.2 Op-amp IC-741 pin diagram.

EXPERIMENT-1

INVERTING AND NON-INVERTING AMPLIFIERS USING OP AMPS

A. INVERTING AMPLIFIER:

Aim: To design and setup an inverting amplifier circuit with OP AMP 741C for a gain of 5, Plot the waveforms, observe the phase reversal, measure the gain.

1.11 APPARATUS:

1. µA-741 OP-AMP
2. Resisters(1KΩ, 5KΩ)
3. Dual power supply
4. Signal generator(0-1MHz)
5. Bread board and connecting wires.
6. CRO

1.12 THEORY:

It is a closed loop mode application of opamp and employs negative feedback. The RfandRiare the feedback and input resistance of the circuit respectively. The input terminals ofthe op-amp draws no current because of the large differential input impedance. The potentialdifference across the input terminals of an opamp is zero because of the large open loop gain.Due to these two conditions, the inverting terminal is at virtual ground potential. So thecurrent flowing through Ri and Rf are the same.

$$I_i = I_f$$

That is Vin/Ri = - Vo /Rf

Therefore Vo/Vin = Av = - Rf/ Ri,

Here the –VE sign indicates that the output will be an amplified wave with 180 degree phase shift

shift (inverted output). By varying the Rf or Ri, the gain of the amplifier can be varied to any desired value.

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1.13 PROCEDURE:

1. Check the components.

2. Setup the circuit on the breadboard and check the connections.

3. Switch on the power supply.

4. Give 1 Vpp / 1 KHz sine wave as input.

5. Observe input and output on the two channels of the oscilloscope simultaneously.

6. Note down and draw the input and output waveforms on the graph.

7. Verify the input and output waveforms are out of phase.

8. Verify the obtained gain is same as designed value of gain.

1.14 Design:

Gain of an inverting amplifier Av = Vo/Vin = - Rf / Ri

The required gain = 5,

That is Av = - Rf/ Ri = 5

Let Ri = 1KΩ, Then Rf = 5KΩ

Observations:

Vin = 1 Vpp

Vo=?

Gain, Av = Vo/Vin =?

Observed phase difference between the input and the output on the CRO =?

RESULT:

1. Theoretical calculations.
2. Practical calculations.

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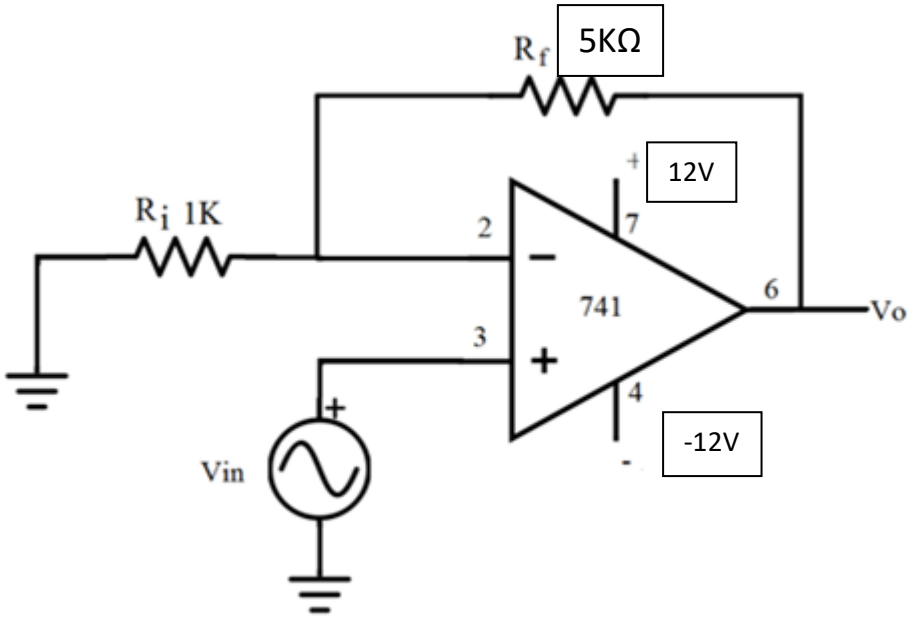

Fig 1.3 Non-inverting amplifier using op-amp IC-741.

Design:

Gain of an non-inverting amplifier Av=Vo/Vin = 1+Rf/ Ri,

Let the required gain be 6,

Therefore Av= 1+Rf/ Ri= 6

Rf/ Ri = 5

Take Ri= 1KΩ, Then Rf = 5KΩ

Observations:

Vin = 1Vpp

Vo = ?

Gain Av = Vo/Vin =?

Observed phase difference between the input and the output on the CRO =?

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B. NON- INVERTING AMPLIFIER:

Aim: To design and setup a non-inverting amplifier circuit with OPAMP IC 741C for a gain of 6, plot the waveform, observe the phase reversal, measure the gain.

1.21 APPARATUS:

1. µA-741 OP-AMP
2. Resisters-(1K, 5K)
3. Dual power supply
4. Signal generator(0-1MHz)
5. Bread board and connecting wires.
6. CRO

1.22 THEORY:

Principle:

It is a linear closed loop mode application of op-amp and employs negative feedback. The R_f and R_i are the feedback and input resistance of the circuit respectively. There will be no phase difference between the output and input. Hence it is called non-inverting amplifier.

$$\mathbf{Av = Vo / Vin = 1+ R_f/ R_i ,}$$

Here the +Ve sign indicates that the output will be an amplified wave in phase with the input. By varying the R_f or R_i, the gain of the amplifier can be varied to any desired value.

1.23 Procedure:

1. Check the components.
2. Setup the circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Give 1 Vpp / 1 KHz sine wave as input.
5. Observe input and output on the two channels of the CRO simultaneously.
6. Note down and draw the input and output waveforms on the graph.
7. Verify the input and output waveforms are in phase.
8. Verify the obtained gain is same as designed value.

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RESULT:

Theoretical calculations.

Gain of an non-inverting amplifier Av=Vo/Vin = 1+Rf/ Ri,

Let the required gain be 6,

Therefore Av= 1+Rf/ Ri= 6

Rf/ Ri = 5

Take Ri= 1KΩ, Then Rf = 5KΩ

Practical calculations.

Observations:

Vin = 1Vpp

Vo = ?

Gain Av = Vo/Vin =?

Observed phase difference between the input and the output on the CRO =?

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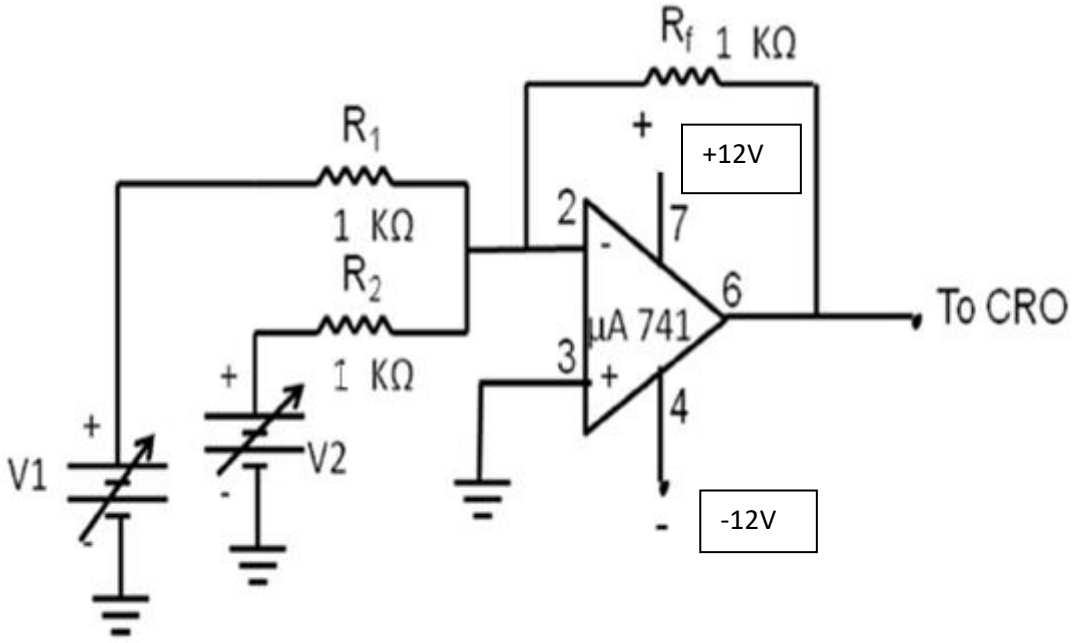

Fig 2.1 Adder design using op-amp IC-741.

Design: $R_f = 1\ k\Omega$ $R_1 = R_2 = 1\ k\Omega$

If $R_1 = R_2 = R_f = R$, then

$$V_0 = -(V_1 + V_2)$$

EXPERIMENT-2

ADDER AND SUBTRACTOR USING OP AMP

AIM: To verify the basic operations of OP-AMP as adder and subtractor.

2.11 APPARATUS:

1. µA-741 OP-AMP
2. Resisters-(1K-3)
3. Dual power supply
4. CRO/Multi-meter.
5. Bread board and connecting wires.

2.12 THEORY:

Adder (Summing Amplifier):

Op-amp may be used to perform summing operation of several input signals in inverting in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively. If the input to the inverting amplifier is increased, the resulting circuit is known as adder.

Output is a linear summation of number of input signals. Each input signal produces a component of the output signal that is completely independent of the other input signal. When there are two inputs i.e. Vo= - (V1+V2) this is the inverted algebraic sum of all the inputs. If we connect the inputs to non inverting terminal then the adder is non inverting adder.

$$V_o = -\left(\frac{Rf}{R1}+V1\frac{Rf}{R2}V2\right) = -(V_1 + V_2)$$

Design: $R_f = 1\ k\Omega \quad R_1 = R_2 = 1\ k\Omega$

If $R_1 = R_2 = R_f = R$, then

$V_0 = -(V_1 + V_2)$

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2.13PROCEDURE:

1. Check the components.
2. Setup the circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Give V1 DC supply.
5. Give V2 DC supply.
6. Make sure that the oscilloscope coupling selector is in the D.C. position.
7. Observe input and output on oscilloscope simultaneously.
8. Measure output voltage using multi-meter.

RESULT:

1. **Theoretical calculations**
2. **Practical calculations.**

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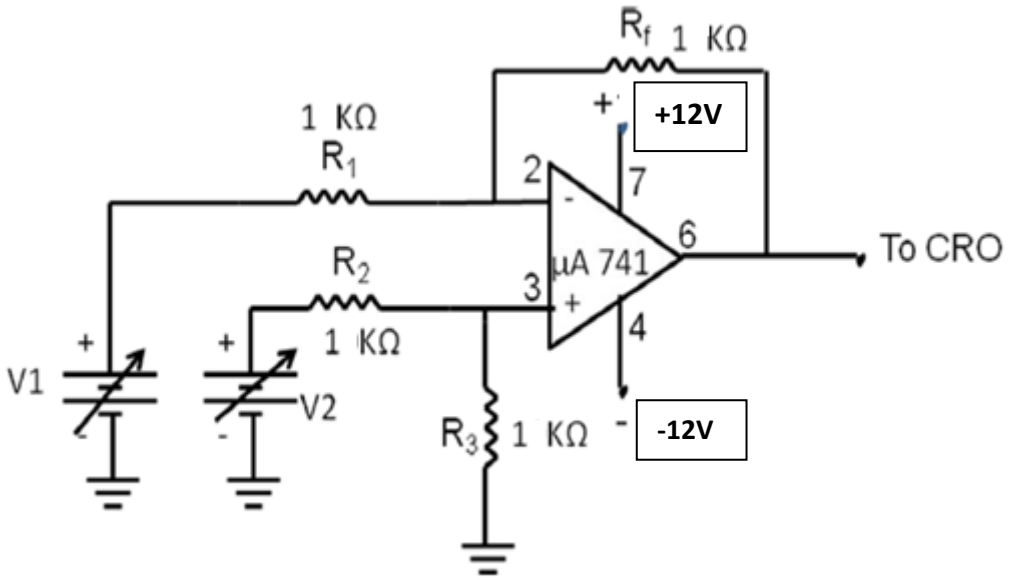

Fig 2.2Subtractordesign using op-amp IC-741.

Design: R_f & R = 1 kΩ, R_1 & R_2 = 1 kΩ

If $R_f = R_1 = R_2 = R$, then $V_0 = V_2 - V_1$

$$V_o = V_2 - V_1$$

SUBSTRACTOR USING OP-AMP:

2.21 APPARATUS:

1. µA-741 OP-AMP.
2. Resisters-(1K-4)
3. Dual power supply.
4. CRO/Multi-meter.
5. Bread board and connecting wires.

2.22 Theory:

A difference amplifier is a circuit that gives the amplified version of the difference of the two inputs, Vo =A(V1-V2), Where V1 and V2 are the inputs and A is the voltage gain. Here input voltage V1 is connected to non-inverting terminal and V2 to the inverting terminal. This is also called as differential amplifier. Output of a differential amplifier can be determined using super position theorem. When V_1=0, the circuit becomes an inverting amplifier with input V_2 and the resulting output is V_{02}= -Rf /Ri (V_2). When V_2=0, the circuit become a non-inverting amplifier with input V_1 and the resulting output is V_{01}= Rf/Ri(V_1). Therefore the resulting output according to super position theorem is

$$Vo = V_{01} + V_{02} = Rf/Ri(V1-V2)$$

2.24 PROCEDURE:

1. Check the components.
2. Setup the circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Give V1 DC supply.
5. Give V2 DC supply.
6. Make sure that the oscilloscope coupling selector is in the D.C. position**.**
7. Observe input and output on oscilloscope simultaneously.
8. Measure output voltage using multi-meter.

RESULT:

1. **Theoretical calculations.**
2. **Practical calculations.**

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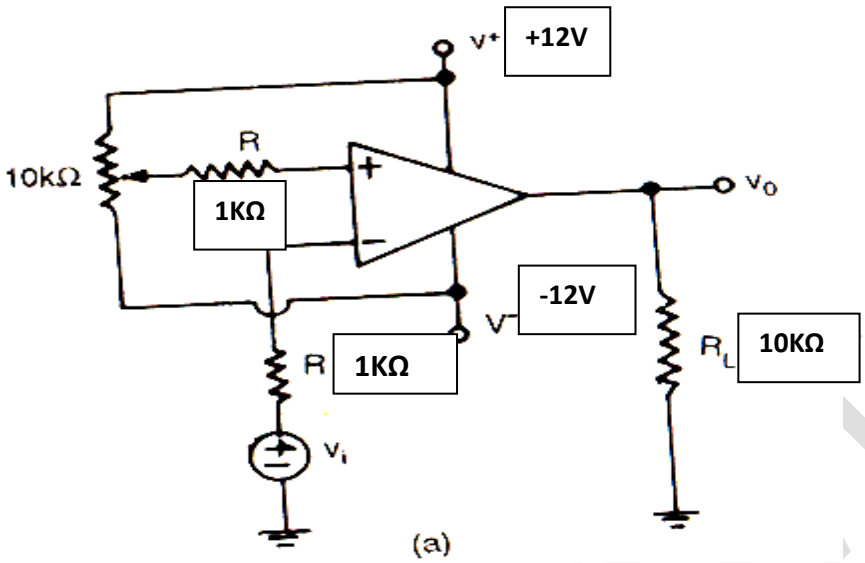

Fig 3.1 Design of Comparator using op-amp IC-741.

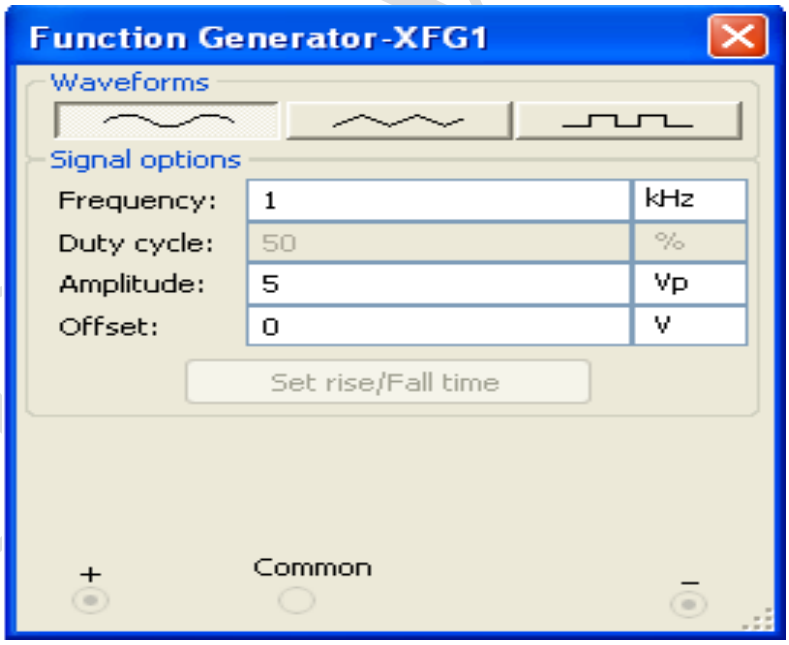

Fig 3.2 Design values for comparator.

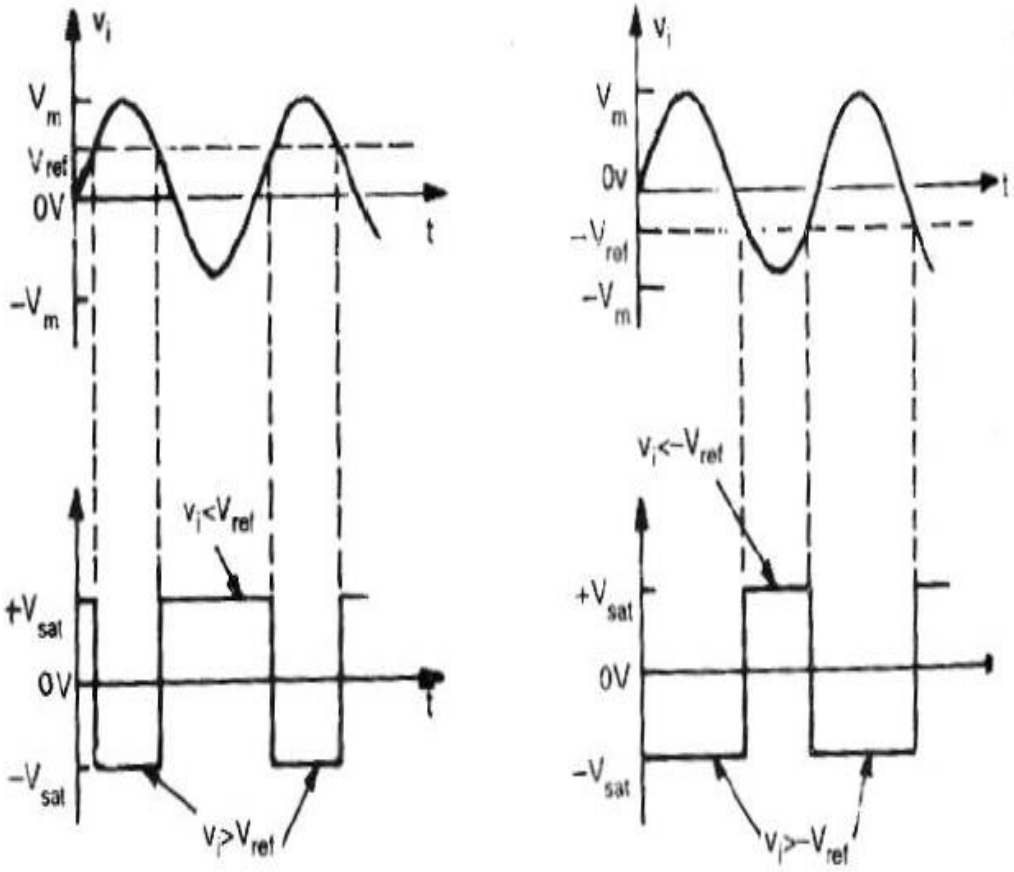

Fig 3.3 Input and output waveform for comparator when V_{ref} is positive and negative.

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EXPERIMENT-3

COMPARATOR USING OP-AMP

AIM: To Study the operation of comparator using OP-AMP IC-741.

3.1 APPARATUS:

1. µA-741 OP-AMP.
2. Resisters-(1KΩ, 1KΩ, 10KΩ)
3. Dual power supply.
4. Pot-(10KΩ)
5. Signal generator.
6. CRO.
7. Bread board and connecting wires.

3.2 Theory

In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output.

When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± VS) has its transfer function typically written as:

$$V_{out} = A_0(V_1 - V_2)$$

However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback) in practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator.

3.3 PROCEDURE:

1. Connect the circuit shown in Fig. And adjust the 10 KΩ potentiometer so thatVref = +0.5V
2. Adjust the signal generator so that vi = 2V pp sine wave at 1 kHz.

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3. Using a CRO observe the input and output waveform simultaneously. Plot theoutput waveform.

4. Adjust the 10 KΩ potentiometer so that Vref = -0.5V. Repeat step 3

3.4 RESULT:

OBSERVATIONS:

V_{out}= _____

V_{in}= _____

Case1: When $V_{ref}$is positive

Observe: square wave output

On time > off time

Case2: When $V_{ref}$is Negative

Observe: square wave output

Off time > on time

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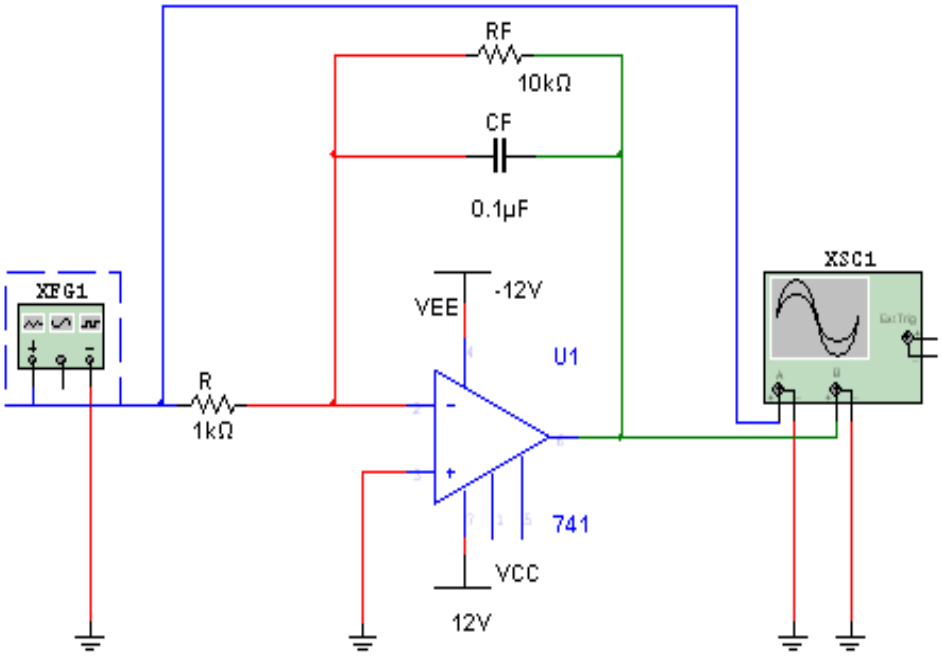

Fig 4.1 Design of integrator using op-amp IC-741.

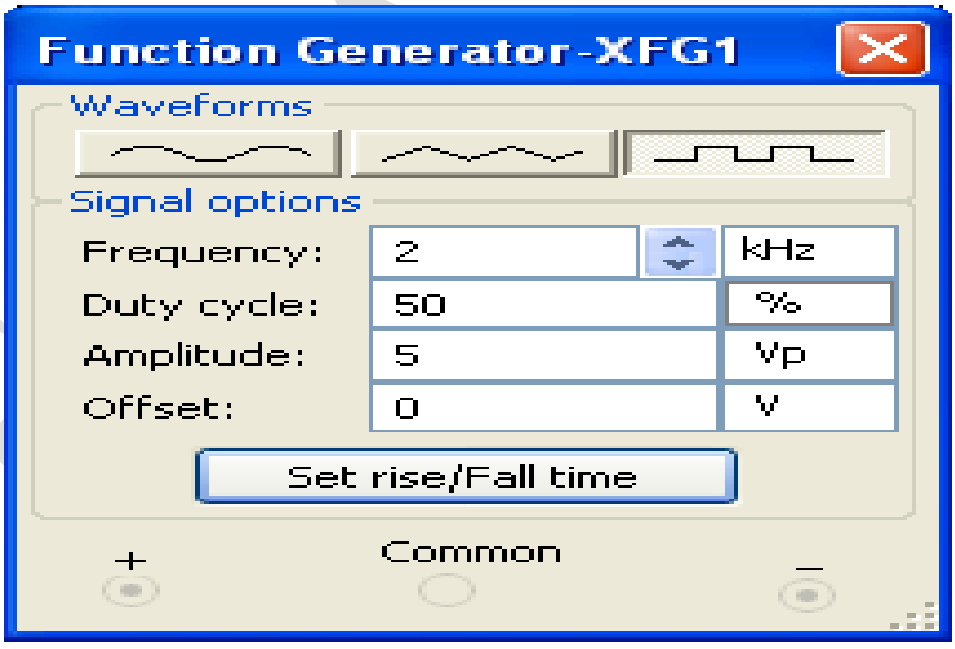

Fig 4.2 Design values for integrator.

EXPERIMENT-4

Integrator Circuit using IC 741

AIM: Design a practical integrator circuit to process input square wave up to 1.5 KHz.

4.1 APPARATUS:

1. CRO
2. Power supply
3. Signal generator
4. Bread board
5. IC-741 OP-AMP
6. Capacitors
7. Registers

4.2 THEORY:

A circuit in which the output waveform is the integral of the input wave is theintegrator. Such a circuit is obtained by using a basic inverting amplifier configuration. If thefeedback resistor Rf is replaced by a capacitor C. The output voltage can be obtained by,

$$V_o = -\frac{1}{RC_f}\int V_{in}\,dt + C$$

Where C is the integration constant and proportional to the value of the output voltage Vo attime t=0 sec. Thus, the output voltage is directly proportional to the negative integral of theinput voltage and inversely proportional to the time constant R Cf. The convenient way tointroduce the AC integration circuit is through frequency response and impedanceconsideration. The transfer function for the true integrator is given by,

$$H(j\omega) = -Zf / Zi = -\frac{1/j\omega c}{R}$$

$$H(j\omega) = -1/j\omega cR$$

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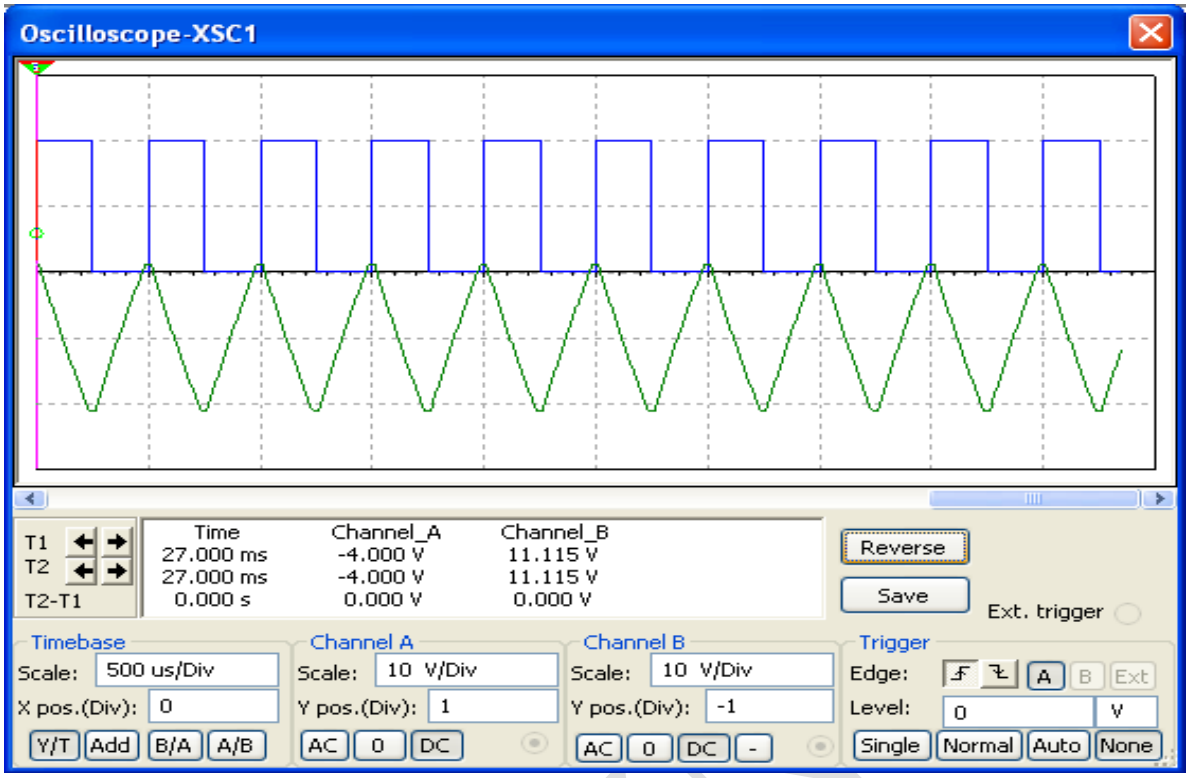

Fig 4.3 Input and output waveform for Integrator when input is square wave

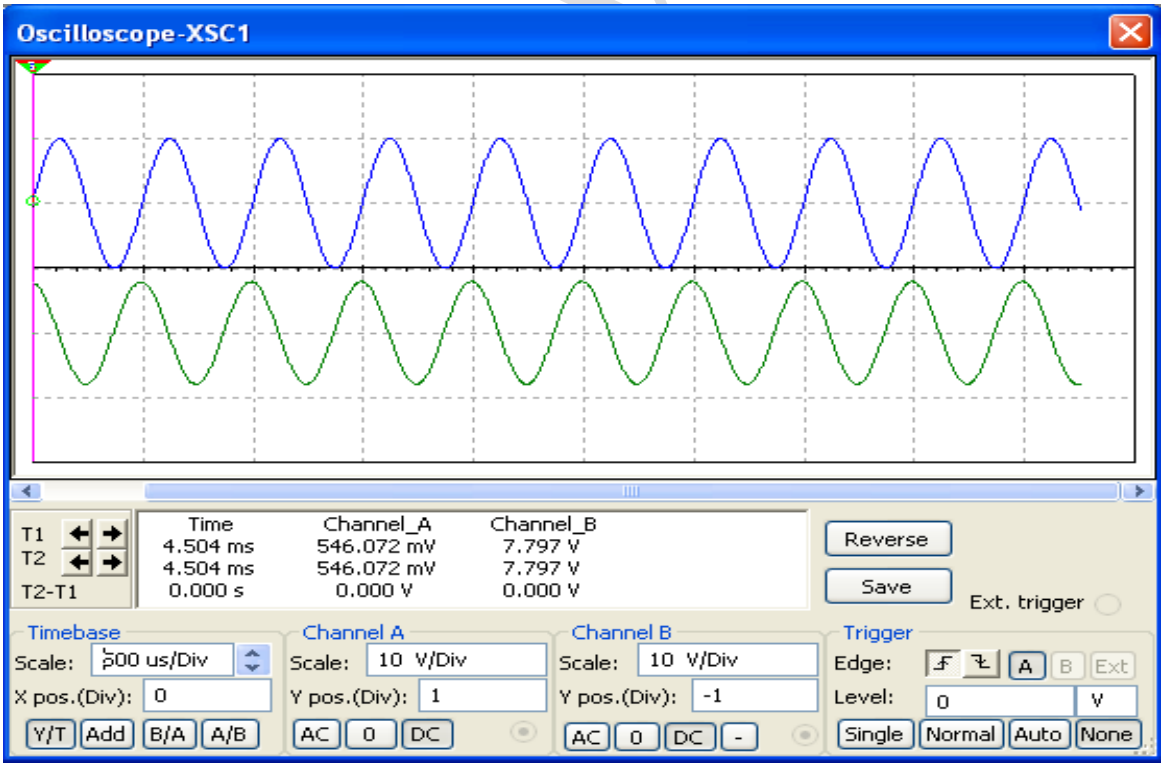

Fig 4.4 Input and output waveform for Integrator when input is

Sine wave

Amplitude response, M (w) =1/wRC It is clear that integration is a form of low pass filteringi.e., the function is very large at low frequency and decreases as the frequency increases.The circuit operates by passing a current that charges or discharges the capacitor overtime. If the op-amp is assumed ideal, nodes *v1* and *v2* are held equal, and so *v2* is a virtualground. The input voltage passes a current through the resistor and series capacitor, whichcharges or discharges the capacitor over time. Because the resistor and capacitor areconnected to a virtual ground, the input current does not vary with capacitor charge and alinear integration operation is achieved.The circuit can be analyzed by applying Kirchhoff's current law at the node *v2*, keeping ideal

$$i_1 = I_B + i_f$$

In an ideal op-amp, $I_B = 0$, so:

$$i_1 = i_f$$

Furthermore, the capacitor has a voltage-current relationship governed by the equation:

$$I_c = C \frac{dV_c}{dt}$$

Substituting the appropriate variables:

$$\frac{V_{in} - V_2}{R_1} = C_F \frac{d(V_2 - V_0)}{dt}$$

In an ideal op-amp, $V2 = V_1 = 0$, resulting in:

$$\frac{V_{in}}{R_1} = C_F \frac{d(V_0)}{dt}$$

Integrating both sides with respect to time:

$$\int_0^t \frac{V_{in}}{R_1} dt = -\int_0^t C_F \frac{dV_0}{dt} dt$$

If the initial value of *vo*is assumed to be 0 V, this results in a DC error of:

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$$V_0 = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt$$

4.3 DESIGN EQUATIONS:

Given f_a= 1.5 KHz;$f_a = \frac{1}{2\pi R_f C_f}$; f_b = 1/ 2πR_1C_f

We know that $f_a = f_b/10$; R_f = 10 R_1; take R_f= 100 KΩ

Find R_1 = 10 KΩ; R_f = 10 R_1

FindC_f = $\frac{1}{2\pi R_f f_a}$ = 1nF; $f_a = \frac{1}{2\pi R_f C_f}$

4.4 PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. Now apply square wave to the circuit.
3. Now vary the time period of the input wave and observe the output.
4. Draw the graph for input and output waveforms.

4.5 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the OP-AMP before connections.
3. Avoid loose contacts.
4. Avoid errors while observing outputs on CRO.

Result: Inputs and outputs of design are verified successfully. According to the input and outputs it is confirmed that, designed integrator works properly.

OBSERVATIONS:

1. The **time period and amplitude of the output waveform**.

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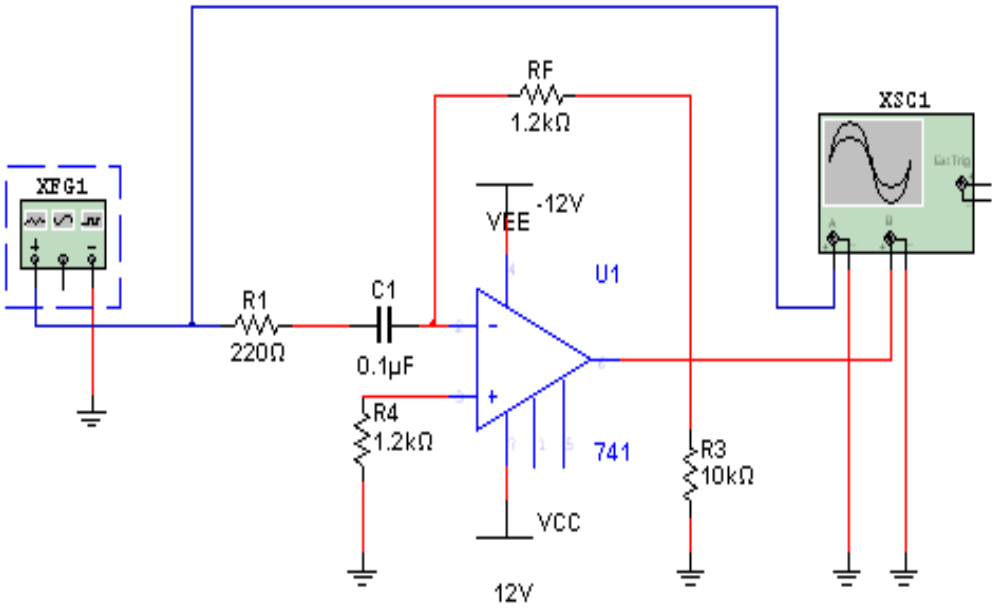

Fig 5.1 Design of differentiator using op-amp IC-741.

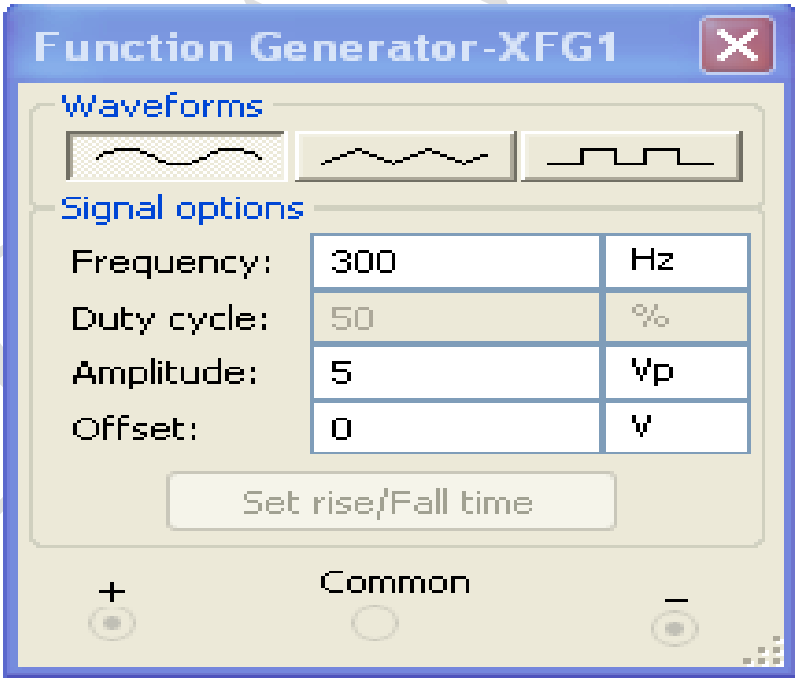

Fig 5.2 Design values for differentiator.

EXPERIMENT-5

Differentiator circuit using Op Amp

AIM: Design a differentiator that differentiate input value with f_{max}= 500Hz.

5.1 APPARATUS:

1. CRO
2. Power supply
3. Signal generator
4. Bread board
5. IC-741 OP-AMP
6. Capacitors
7. Resistors

5.2. THEORY:

Differentiator circuits as its name implies, performs the mathematical operation of differentiator, that is, the output waveform is the derivative of the input. The differentiator may be constructed from a basic inverting amplifier when an input resistor R1 is replaced by a capacitor C,

$$Vo= -Rf\ C\ d\ Vin\ /dt$$

Thus, the output Vo is equal to the Rf C times the negative instantaneous rate of change of the input voltage Vin with time. The right-hand side of the capacitor is held to a voltage of 0 volts, due to the "virtual ground" effect. Therefore, current "through" the capacitor is solely due to changein the input voltage. A steady input voltage won't cause a current through C, but a changinginput voltage will. Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the op-amp. Conversely, a linear, negative rate of input voltage change will result in a steady positive voltage at the output of the op-amp. This polarity inversion from input to output is due to the fact that the input signal is being sent (essentially) to the inverting input of the op-amp, so it

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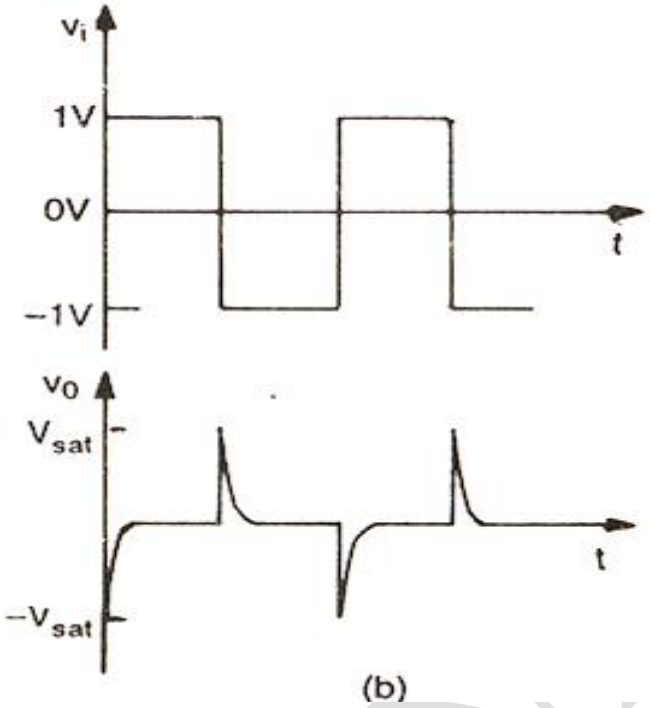

Fig 5.3 Input and output waveform for differentiator when input is square wave.

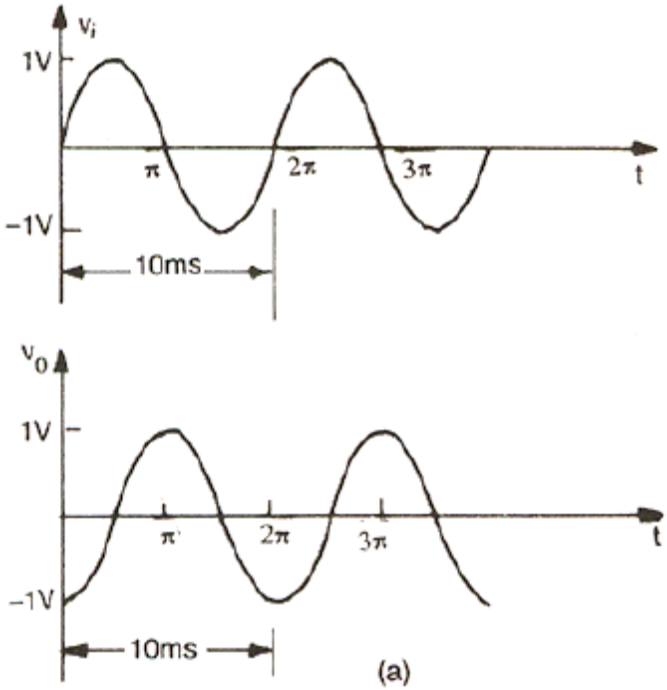

Fig 5.4 Input and output waveform for differentiator when input is

Sine wave .

acts like the inverting amplifier mentioned previously.The faster the rate of voltage change at the input (either positive or negative), the greater the voltage at the output.

The formula for determining voltage output for the differentiator is as follows:

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

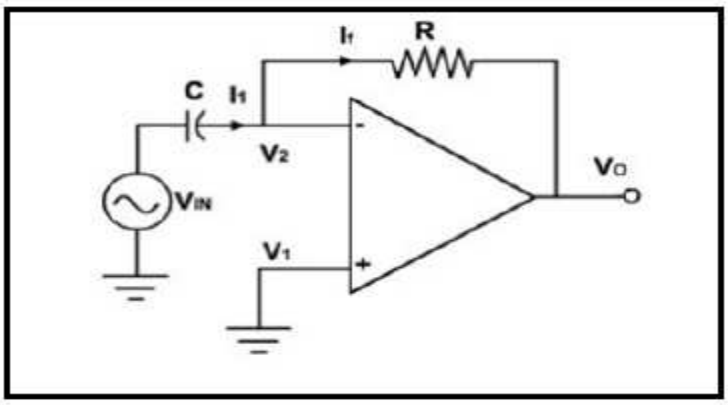

Fig 5.5 Circuit diagram for differentiator

5.3 DESIGN EQUATIONS:

Given f_a= 500Hz, assumeC_1= 0.22µF.

Calculate $R_f = \frac{1}{2\pi f_a C1}$; $f_a = \frac{1}{2\pi RC1}$; R_f = 1.4 KΩ

Choose $f_b = 20\ f_a$; $f_a = \frac{1}{2\pi R_1 C_1}$

Calculate value of$R_1 = \frac{1}{2\pi f_b C_1}$, R_1= 10KΩ

Calculate value of$C_f = \frac{R_1 C_1}{R_f}$, $R_1C_1 = R_fC_f$= 0.01µF

5.4PROCEDURE:

1. At very first connections are made as per the circuit diagram.
2. Now apply square wave as input for the circuit.
3. At this time, vary the time period of the input waveform and observe the output.
4. Draw the graph, for input and output waveforms.

5.5PRECAUTIONS:

1. Keep current-knob of power supply in max position.
2. Check the OP-AMP, before connections.
3. Avoid loose contacts.
4. Avoid error while observing output in CRO.

RESULT:

The input and output waveforms of differentiator are verified successfully. The designed differentiatordifferentiates input correctly.

OBSERVATIONS:

The time period and amplitude of the output waveform of differentiator circuit.

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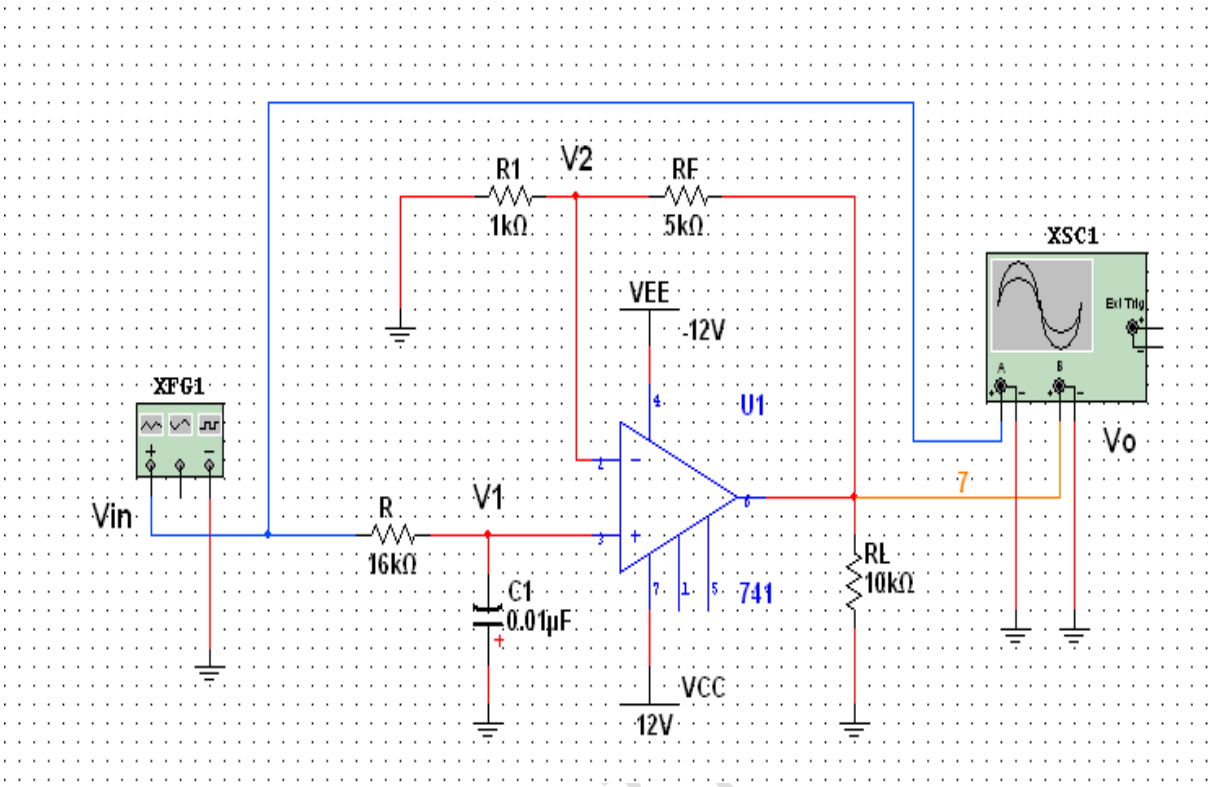

Fig 6.1 Design of low pass filter at cut-off frequency using OP-AMP IC-741.

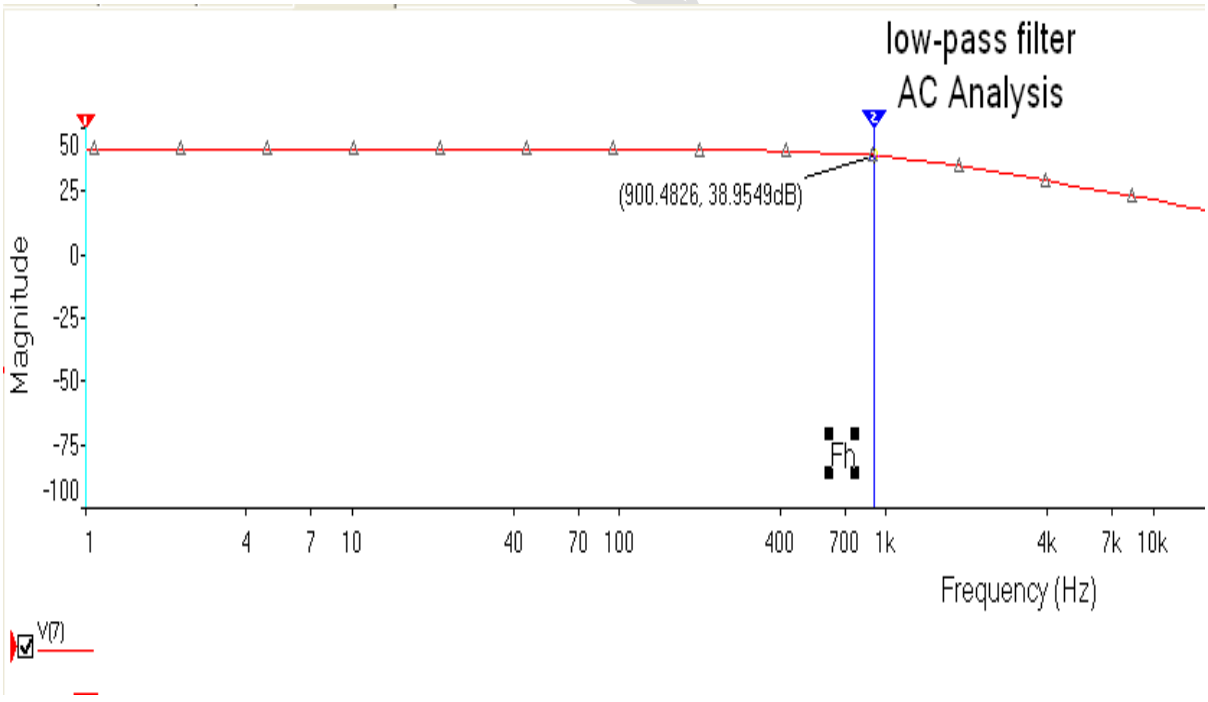

Fig 6.2Magnitude response with respect to frequency for design of low pass filter at cut-off frequency.

EXPERIMENT-6

ACTIVE FILTER APPLICATIONS

A. First order low-pass butter worth filter

AIM: Design a low-pass filter at a cutoff frequency of 1 KHz with a pass band gain of 6. Plot the frequency response of low pass filter.

6.11APPARATUS:

1. IC-741 OP-AMP
2. Resisters
3. Capacitors
4. RPS
5. Signal generator
6. CRO
7. Bread board

6.12 DESIGN EQUATIONS:

Given that $\mathbf{f_h = 1KHz, A_F = 6;}$

Let $\mathbf{C = 0.01\mu F}$; calculate $\mathbf{R = \frac{1}{2\pi f_h C} = 15.91K\Omega;}$

Select $\mathbf{R_1 = 1K\Omega;}$

Find $\mathbf{R_f = 5R_1}$; since $\mathbf{A_f = 1 + \frac{R_F}{R_1};}$

6.13 PROCEDURE:

1. Design the circuit as per the given specifications. All the Connections are made as per the circuit diagram.
2. Now set V_{in} = 1V, by using signal generator.
3. In this step, keep input voltage constant. Now vary the frequency from 0Hz to 20 KHz.
4. Determine higher cut-off frequency.
5. Finally, plot a graph of voltage gain versus frequency.

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Frequency F(Hz) V_{in}= 1V	Output voltage V_o(V)	Gain magnitude (V_o/V_{in})	Magnitude in db 20log(V_o/V_{in})
10	6	6	15.56
300	6	6	15.56
50	6	6	15.16
100	6	6	15.56
350	5.8	5.8	15.56
500	5.4	5.4	14.64
600	5.2	5.2	14.32
800	4.6	4.6	13.25
1K	4.4	4.4	12.86
2K	2.4	2.4	7.60
5K	1.4	1.4	2.92
10K	0.7	0.7	-3.09
20K	0.4	0.4	-7.95

Fig 6.3 Magnitude response with respect to frequency for design of low pass filter at cut-off frequency.

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6.14 CALCULATIONS

1. **Theoretical calculations,**

   i. $\mathbf{f_h = \frac{1}{2\pi RC} = 1\ KHz;}$

   ii. $\mathbf{A_F = 1 + \frac{R_F}{R_1} = 6;}$

2. **Practical calculations,**

   i. $\mathbf{f_h = 900\ HZ;}$

   ii. $\mathbf{A_F = 6;}$

RESULT:

The low-pass filter is designed according to given specifications and finally frequency response curve is drawn.

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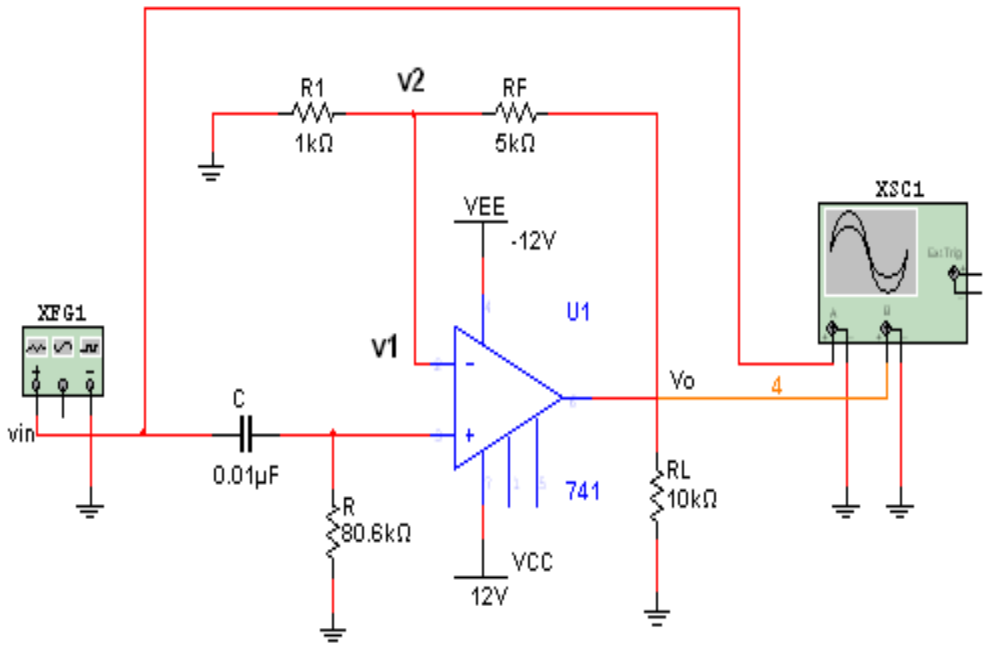

Fig 6.4 Design of High-pass filter at cut-off frequency using OP-AMP IC-741.

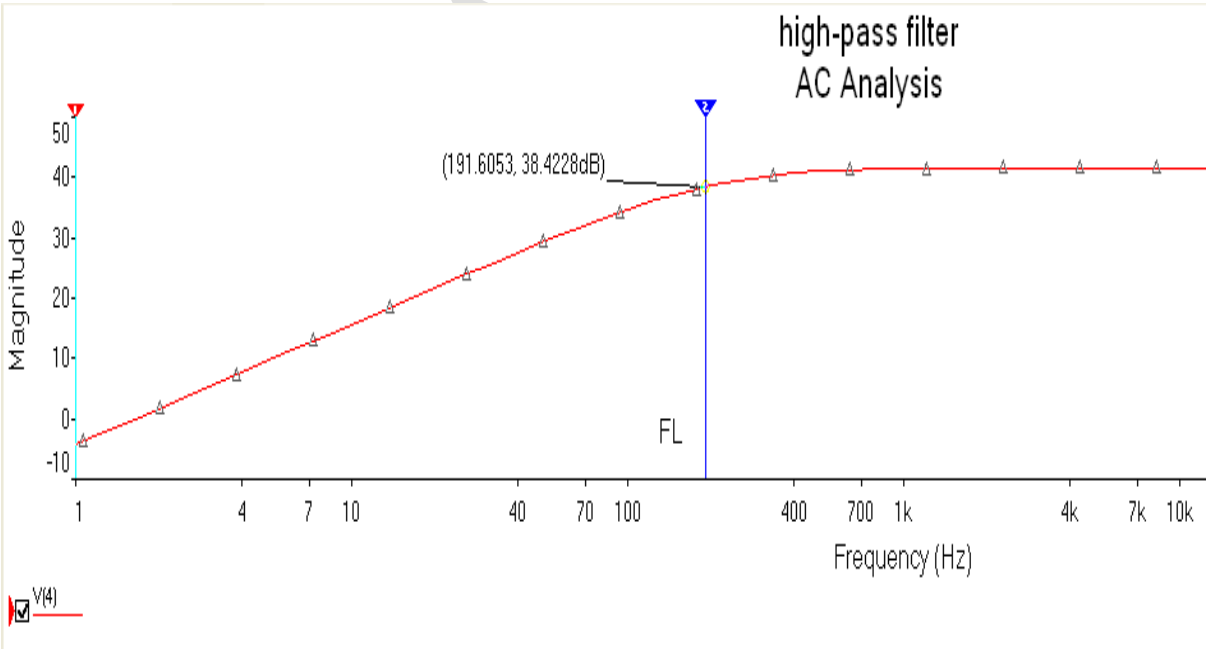

Fig 6.5Magnitude response with respect to frequency for design of High-pass filter at cut-off frequency

B. First order high-pass Butter worth filter.

AIM: Design a high-pass filter at a cut-off frequency of 200 Hz with a pass-band gain of 6 and then plot the frequency response curve for the designed filter.

3.21 APPARATUS:

1. IC-741 OP-AMP
2. RPS
3. CRO
4. Signal generator
5. Resisters
6. Capacitors
7. Bread board

3.22 DESIGN EQUATIONS:

Given, $\mathbf{f_L = 200\ Hz;\ A_f = 6;}$

Let C = 0.01 µF;

Calculate, $\mathbf{R = \frac{1}{2\pi f_L C} = 79.57\ K\Omega}$

$\mathbf{f_L = \frac{1}{2\pi RC}}$

Select, R_1 = 1 KΩ

Determine $R_f = 5R_1$, where $\mathbf{A_F = 1 + \frac{R_f}{R_1}}$

3.23 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are done as per the circuit diagram.
2. Now set V_{in} = 1V, by using signal generator.
3. In this step, keep input voltage constant. Now vary the frequency from 0Hz to 20 KHz.
4. Determine lower cut-off frequency.
5. Finally, plot a graph of voltage gain versus frequency.

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Frequency F(Hz) V_{in}= 1V	Output voltage V_o(V)	Gain magnitude (V_o/V_{in})	Magnitude in db 20log(V_o/V_{in})
30	1	1	0
50	1.6	1.6	4.08
100	2.8	2.8	8.94
150	3.6	3.6	11.12
200	4.4	4.4	12.86
250	4.8	4.8	13.62
300	5	5	13.97
400	5.2	5.2	14.32
600	5.6	5.6	14.96
800	5.8	5.8	15.26
1K	5.9	5.9	15.41
1.5K	6	6	15.56
2K	6	6	15.16
5K	6	6	15.56
20K	6	6	15.56

Fig 6.6 Magnitude response with respect to frequency for design of High-pass filter at cut-off frequency

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3.24 CALCULATIONS:

1. **Theoretical calculations,**

   i. $\mathbf{f_L = \frac{1}{2\pi RC} = 200\ KHz;}$

   ii. $\mathbf{A_f = 1 + \frac{R_f}{R_1} = 6;}$

2. **Practical calculations,**

   i. $\mathbf{f_L = 190\ Hz}$

   ii. $\mathbf{A_f = 6}$

3.24 RESULT:

The high-pass filter is designed according to given specifications and finally frequency response curve is drawn.

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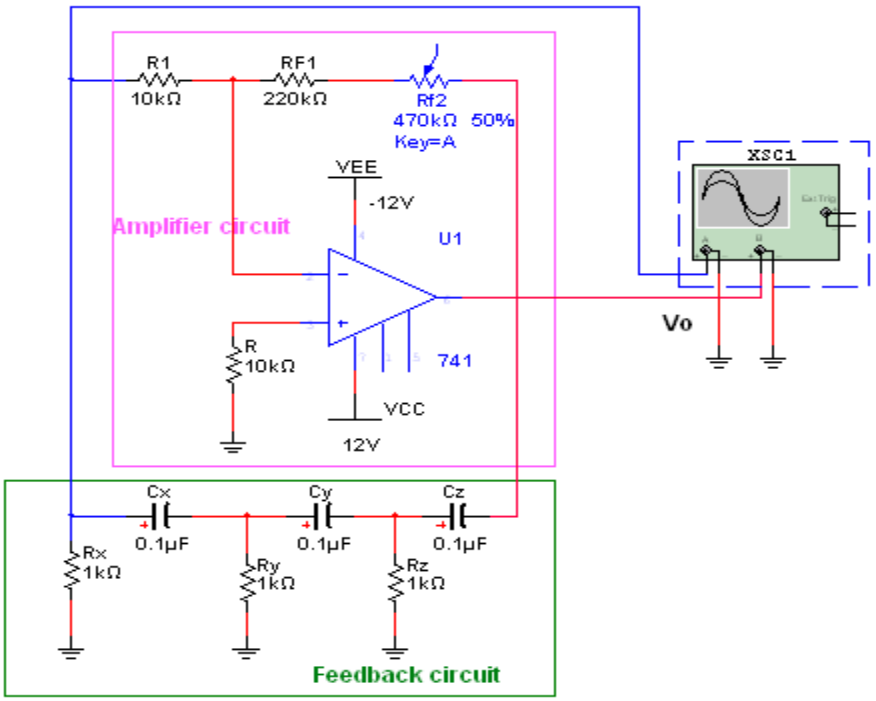

Fig 7.1 Design of phase-shift oscillator using OP-AMP IC-741.

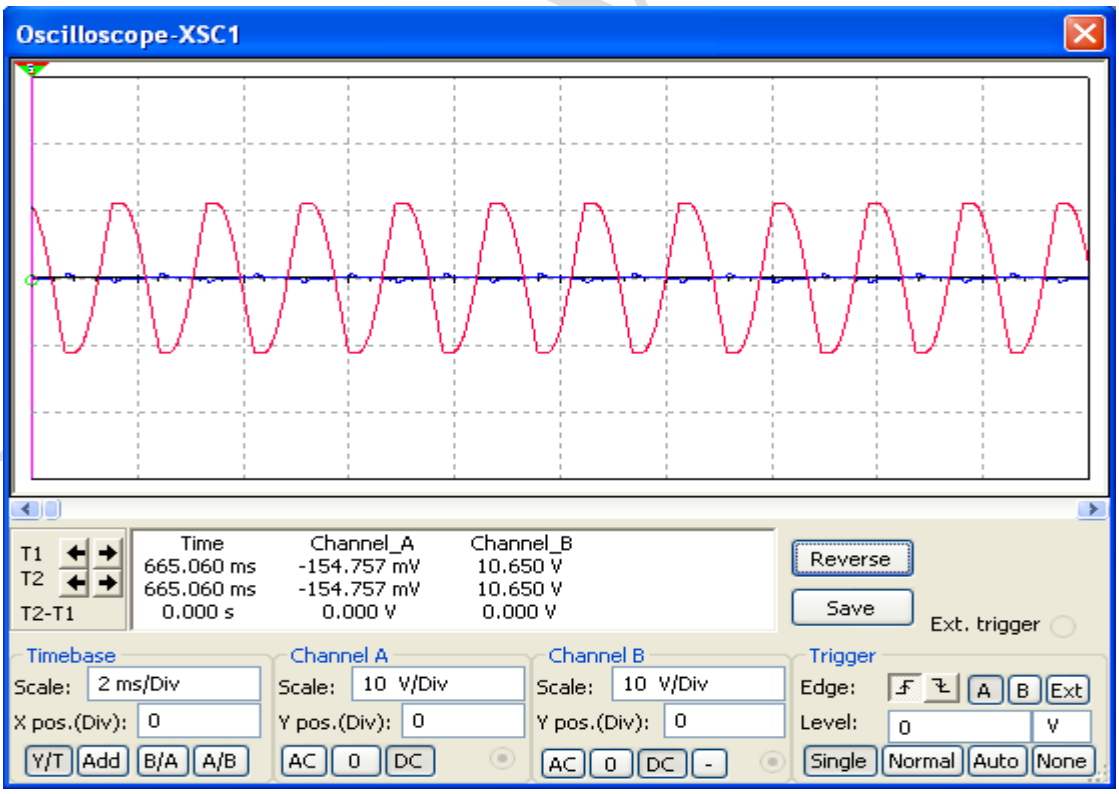

Fig 7.2 output sine wave for design of phase-shift oscillator using OP-AMP IC-741.

EXPERIMENT-7

IC 741 Waveform Generators – Sine, Square wave and Triangular waves

A. Sine wave generator:

AIM: Design a phase-shift oscillator with f_0 = 650 Hz..Observe the output wave form i.e. sine wave and determine frequency of oscillations.

7.11 APPARATUS:

1. IC-µA 741
2. RPS
3. CRO
4. Resisters
5. Capacitors
6. Pot
7. Bread board

7.12 DESIGN EQUATIONS:

Given, f_0 = 650 Hz; C = 0.1µF

$$\mathbf{f_0 = \frac{1}{2\pi RC\sqrt{6}} = \frac{0.065}{RC}}$$

$$\mathbf{R = \frac{0.065}{f_0\, C} = 1\ K\Omega}$$

It is necessary to take R_1 = 10R =10 KΩ (To prevent loading of the amplifier because of RC networks)

$$\mathbf{R_F = 29R_1,\ because\ A_v = \frac{1}{\beta} = 29,\ hence\ A_v \geq 29}$$

$$\mathbf{= 29\ K\Omega}$$

To set R_1 valve choose pot i.e. pot $R_{OM} = R_1$

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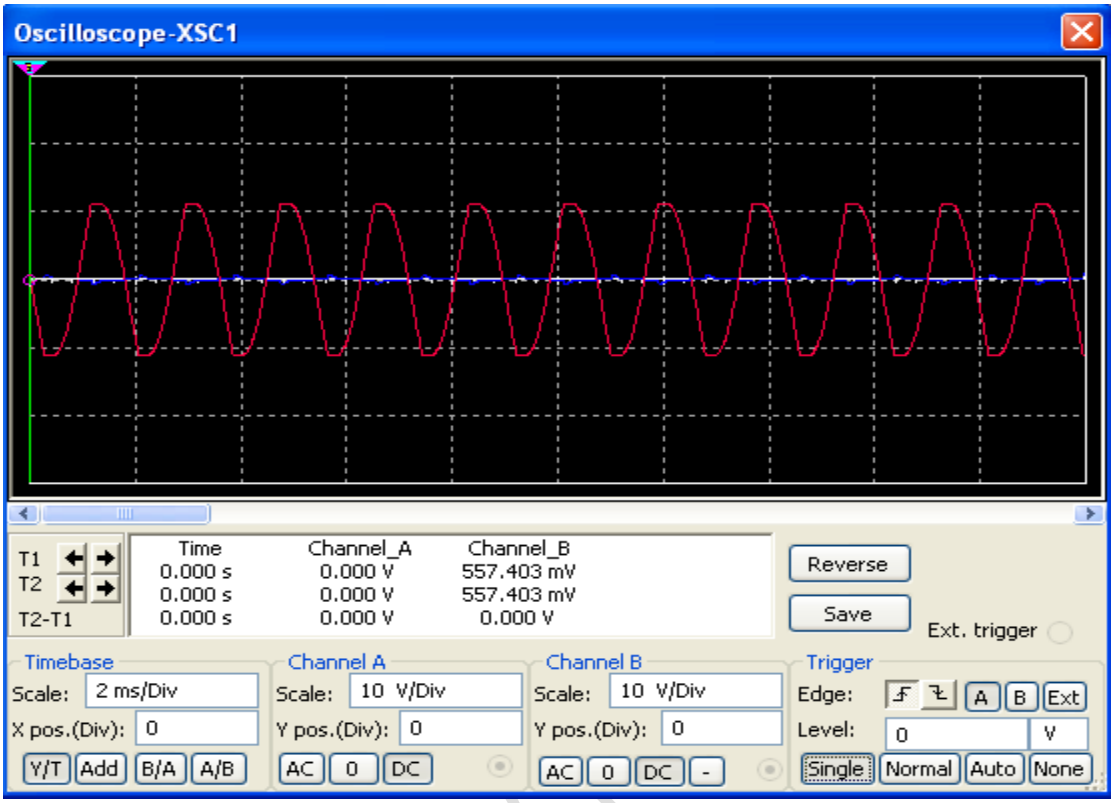

Fig 7.3 output sine wave for design of phase-shift oscillator using OP-AMP IC-741.

7.13 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Now vary the potentiometer of value 470 KΩ slowly until you get a stable sinusoidal wave on the CRO screen.
3. The output wave form is noted at 6th pin of IC-µA741 OP-AMP on CRO.
4. Now calculate the frequency of the waveform.
5. Finally draw the graph for output waveform.

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7.14 CALCULATIONS:

1. **Theoretical calculations,**

$$f_0 = \frac{1}{2\pi RC\sqrt{6}} = \frac{0.065}{RC}$$

Gain = $\frac{R_F}{R_1}$ = 29

Where R_f = 220K + pot value

= 290kΩ

The value of the pot is measured by multi-meter = 70 KΩ (when pot connections are removed from the kit)

2. **Practical calculations,**

$$f_0 = 625 \text{ Hz}$$

$$\text{Gain} = \frac{R_f}{R_1} = \frac{220K+Pot}{R_1} = 29$$

7.15 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the OP-AMP before connections.
3. Avoid loose contacts.
4. Avoid errors while observing outputs on CRO.

RESULT:

The Phase-shift oscillator is designed according to given specifications. Experimental observation on CRO shows sinusoidal waveform and finally frequency of oscillation is calculated for output waveform.

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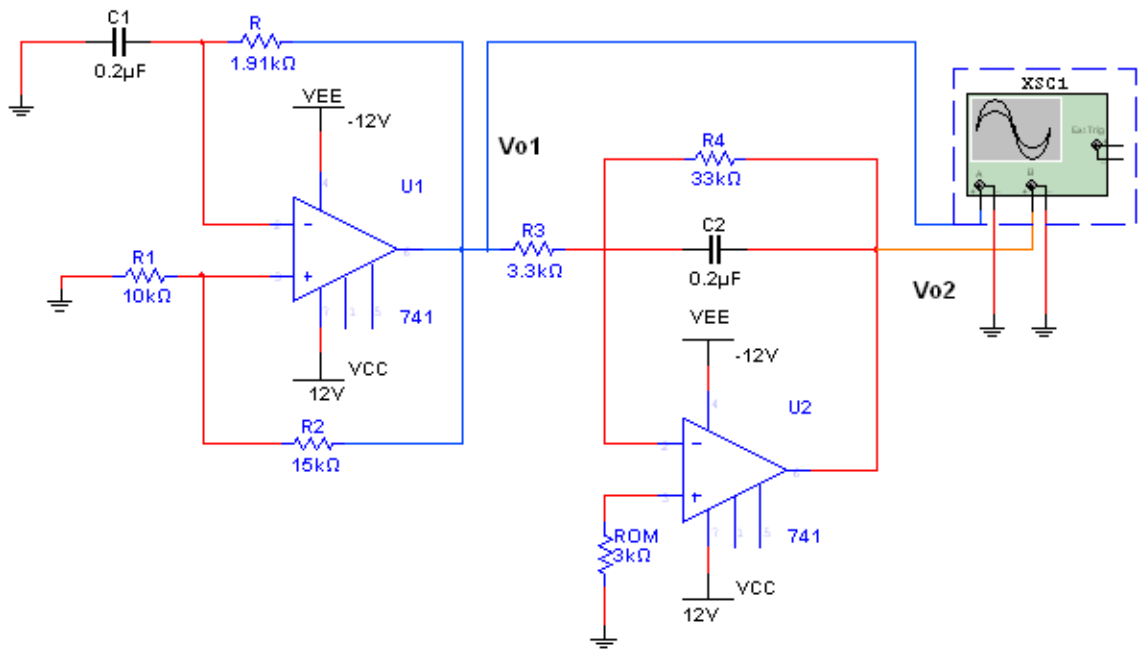

Fig 7.4 Triangular wave generator.

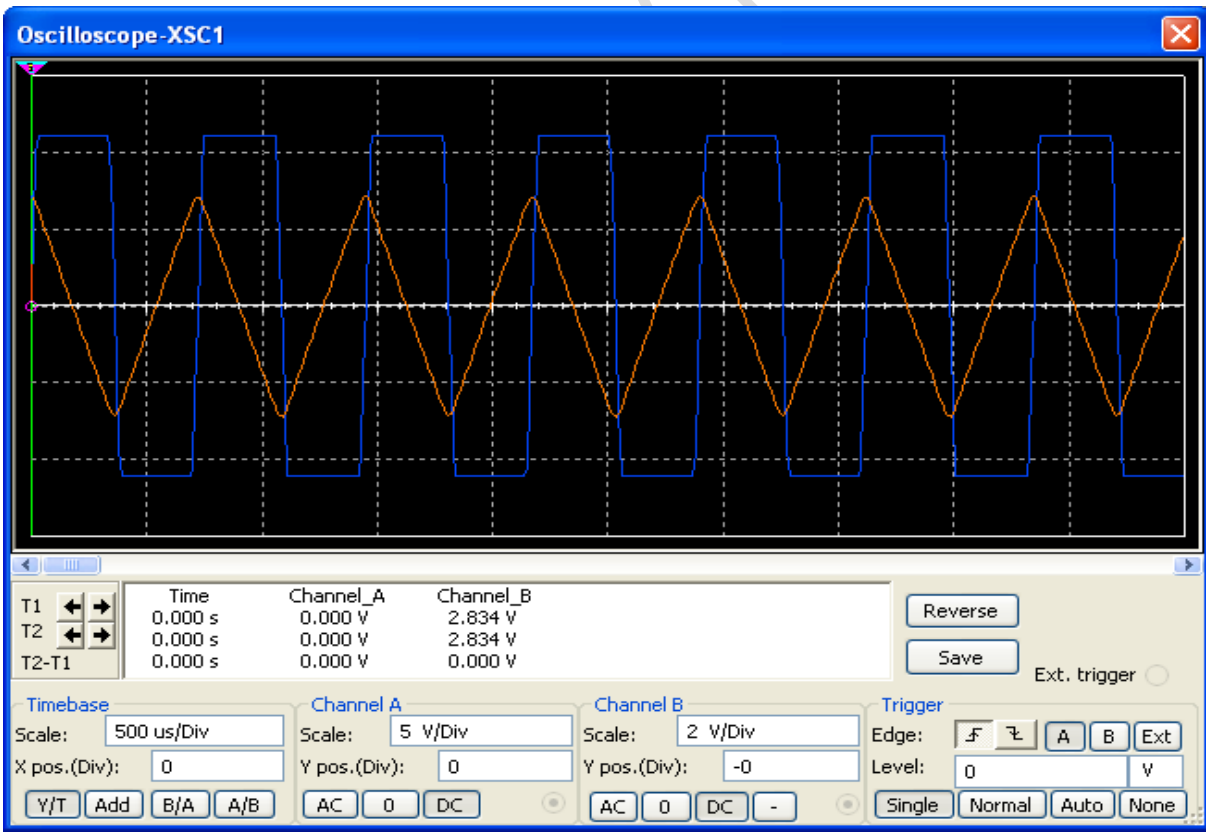

Fig 7.5Output of Triangular wave generator.

B. Triangular wave generator

AIM: Construct a function generator to generate triangular wave with f_0 = 1.5 KHz. Observe the output wave form i.e. triangular wave and determine frequency of oscillations.

7.21 APPARATUS:

1. IC-µA 741 or IC-HA741-2
2. RPS
3. CRO
4. Resisters
5. Capacitors
6. Pot
7. Bread board

7.22 DESIGN EQUATIONS:

Triangular wave generator:

$5R_3C_2 > \frac{T}{2}$ (Where T is the time period of the input wave)

But $R_3C_2 = T$(for stable triangular wave)

Choose $C_2 = 0.2\mu F$

$R_3 = \frac{T}{C_2} = 3.33\ K\Omega$

Find $R_4 = 10R_3 = 33\ K\Omega$

Keep $R_{OM} = R_3 = 3.33\ K\Omega$

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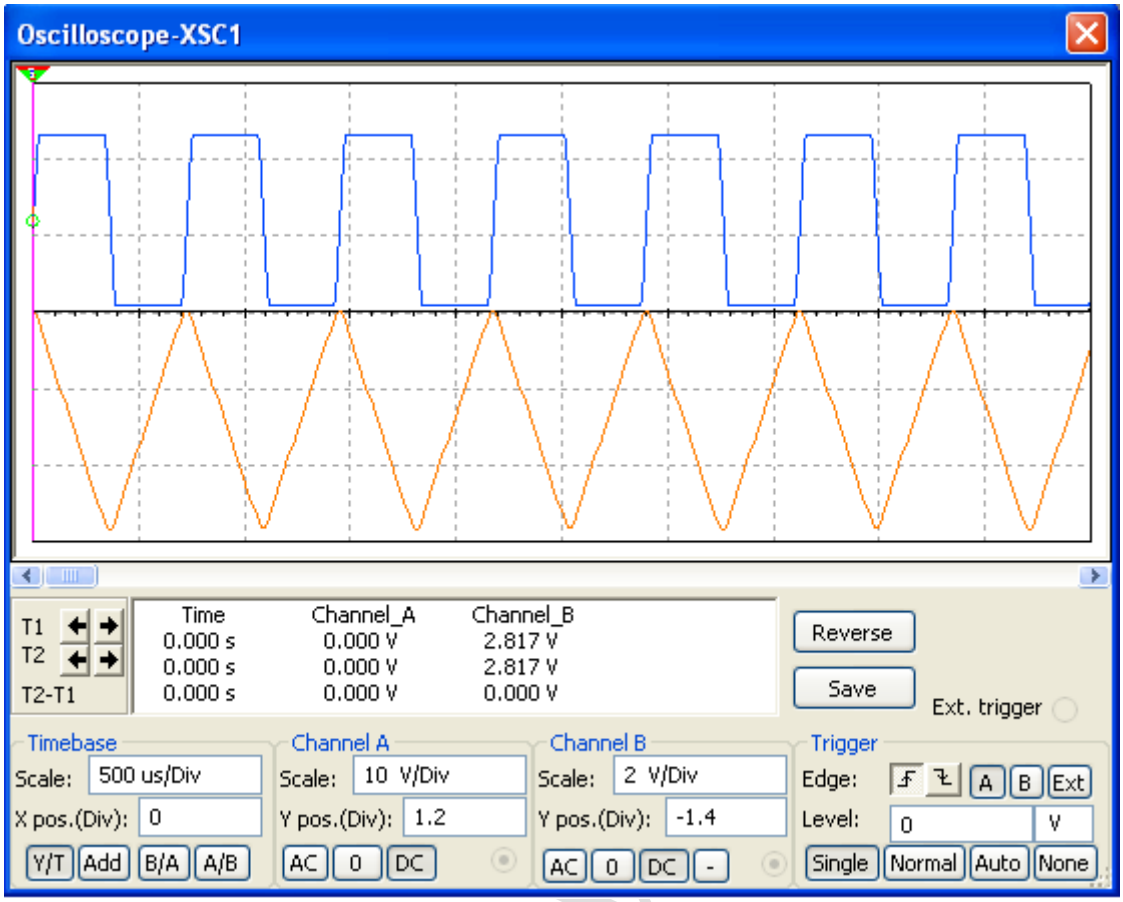

Fig 7.6 Output of Triangular wave generator.

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7.23 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Now take a short look on CRO for experimental observation,
    a. Output waveform V_o' at A_1(pin 6)
    b. Triangular waveform V_o at A_2(pin 6)
3. Measure amplitude and frequency.
4. Finally plot all the waveforms on graph sheet.
5. Output voltage of triangular wave
    a. v_0 = 2.3 V
    b. Frequency f_0 = 1.53 KHz

7.24 RESULT:

The signal generator is designed according to given specifications. Experimental observation on CRO shows triangular waveform and finally frequency of oscillation is calculated for output waveform.

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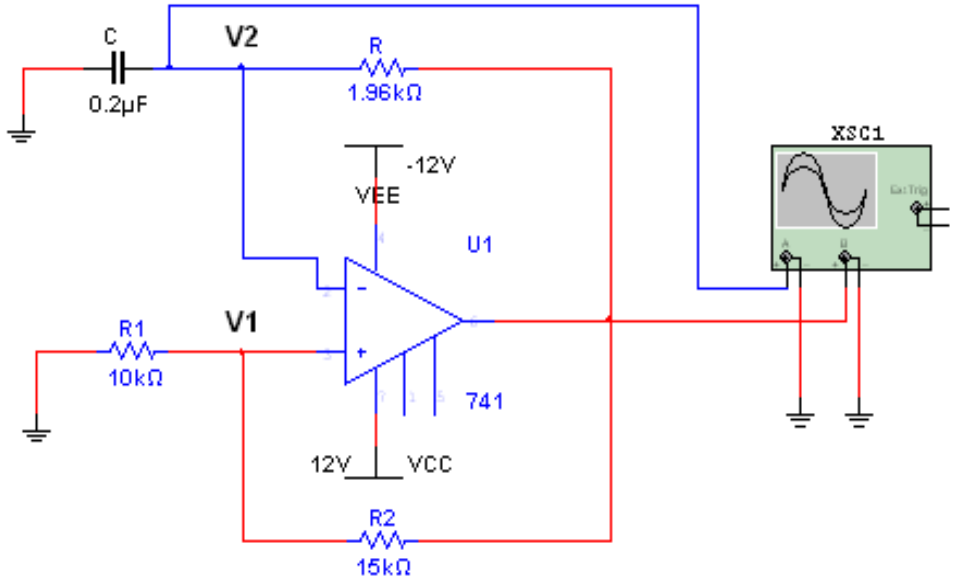

Fig 7.7 Square wave generator

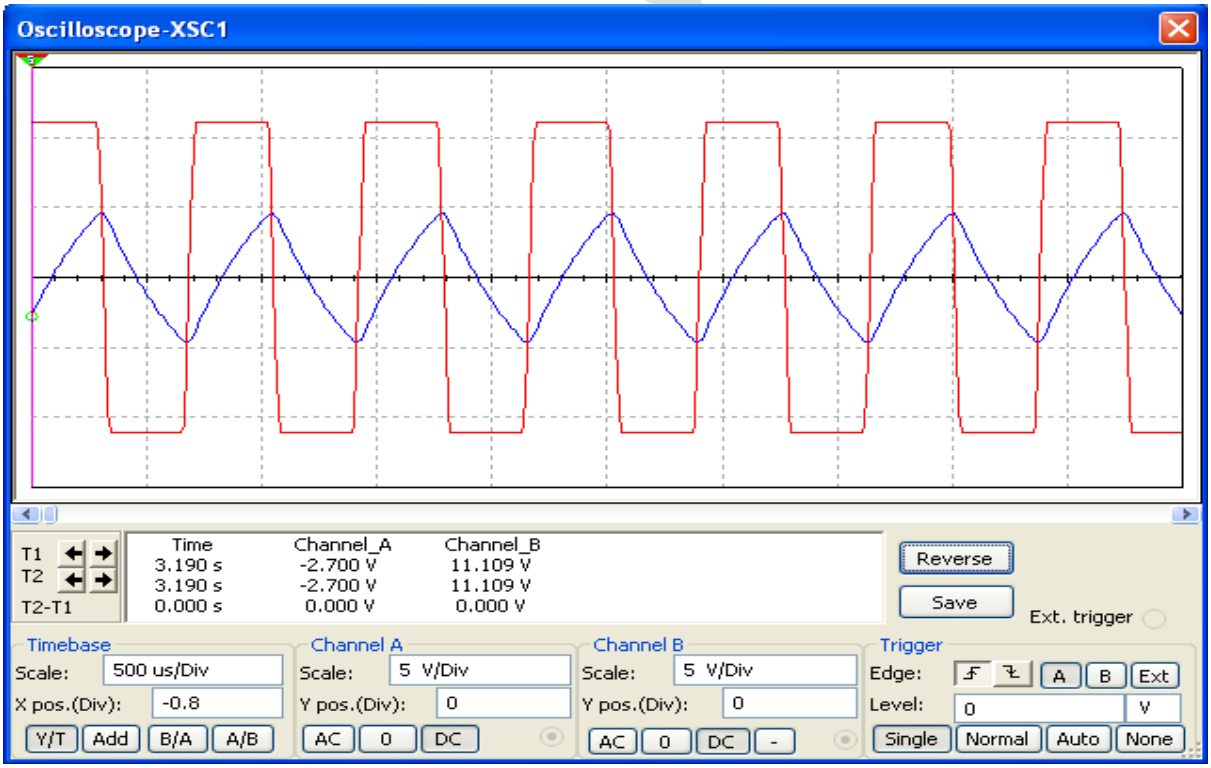

Fig 7.8 Ouput of Square wave generator.

C. Square wave generator

AIM: Construct a function generator to generate square wave with f_0 = 1.5 KHz. Observe the output wave form i.e. square wave and determine frequency of oscillations.

7.31 APPARATUS:

1. IC-µA 741 or IC-HA741-2
2. RPS
3. CRO
4. Resisters
5. Capacitors
6. Pot
7. Bread board

7.32 DESIGN EQUATIONS:

Square wave generator:

Given, f_0 = 1.5 KHz

Choose R_1 = 10 KΩ, R_2 = 15 KΩ, C = 0.2 µF

Calculate R = $\frac{1}{2\pi f_0 C \ln[(2R_1+R_2)/R_2]}$ = 1.9 KΩ

7.33 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Now take a short look on CRO for experimental observation,
   a. Output waveform(pin 6)
   b. Capacitor voltage waveform(pin 2)
3. Measure amplitude and frequency.
4. Finally plot all the waveforms on graph sheet.
5. Output voltage of square wave v_0' = 11 V,

Frequency f_0 = 1.53 KHz,

Voltage across capacitor = 4V

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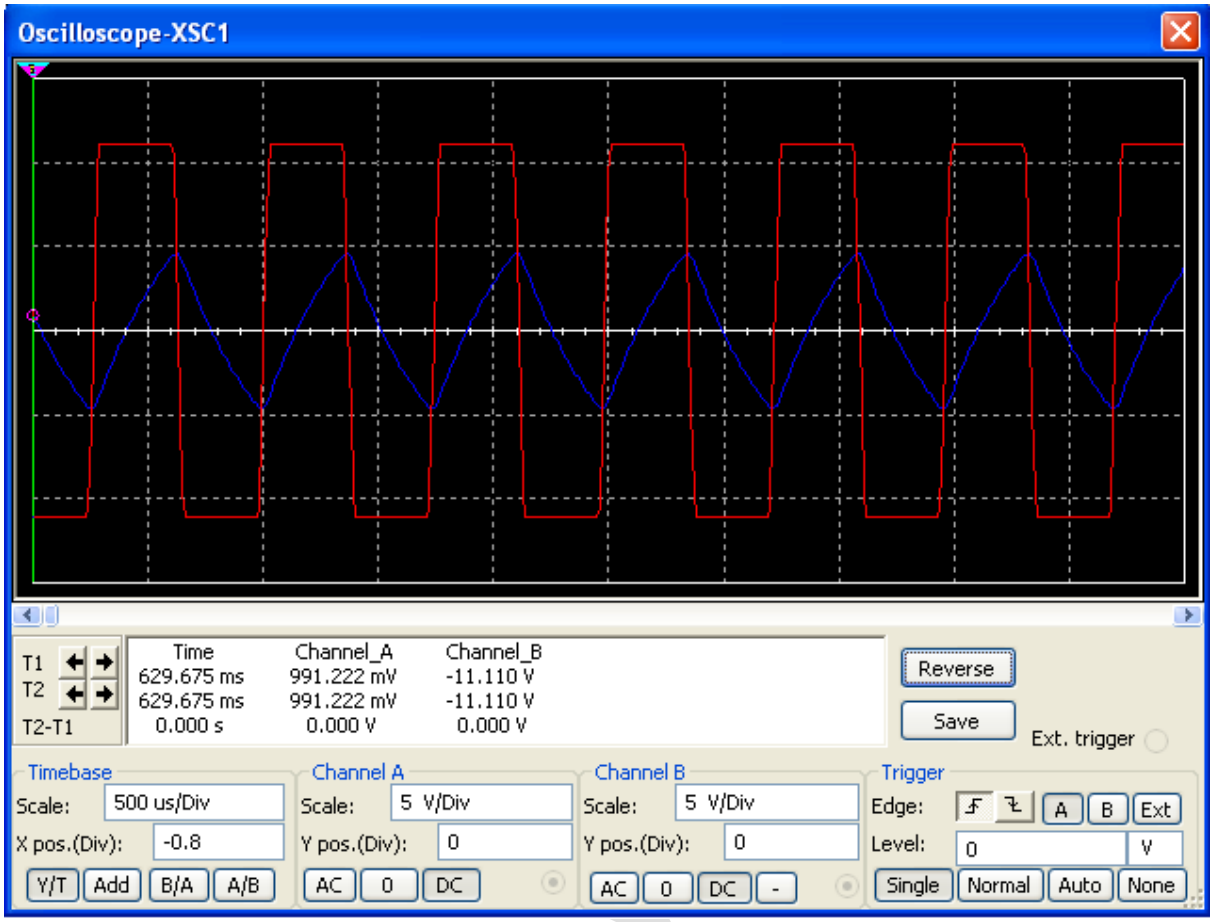

Fig 7.9 Ouput of square wave generator.

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7.34 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the OP-AMP before connections.
3. Avoid loose contacts.
4. Avoid errors while observing outputs on CRO.

RESULT:

The signal generator is designed according to given specifications. Experimental observation on CRO shows square waveform and finally frequency of oscillation is calculated for output waveform.

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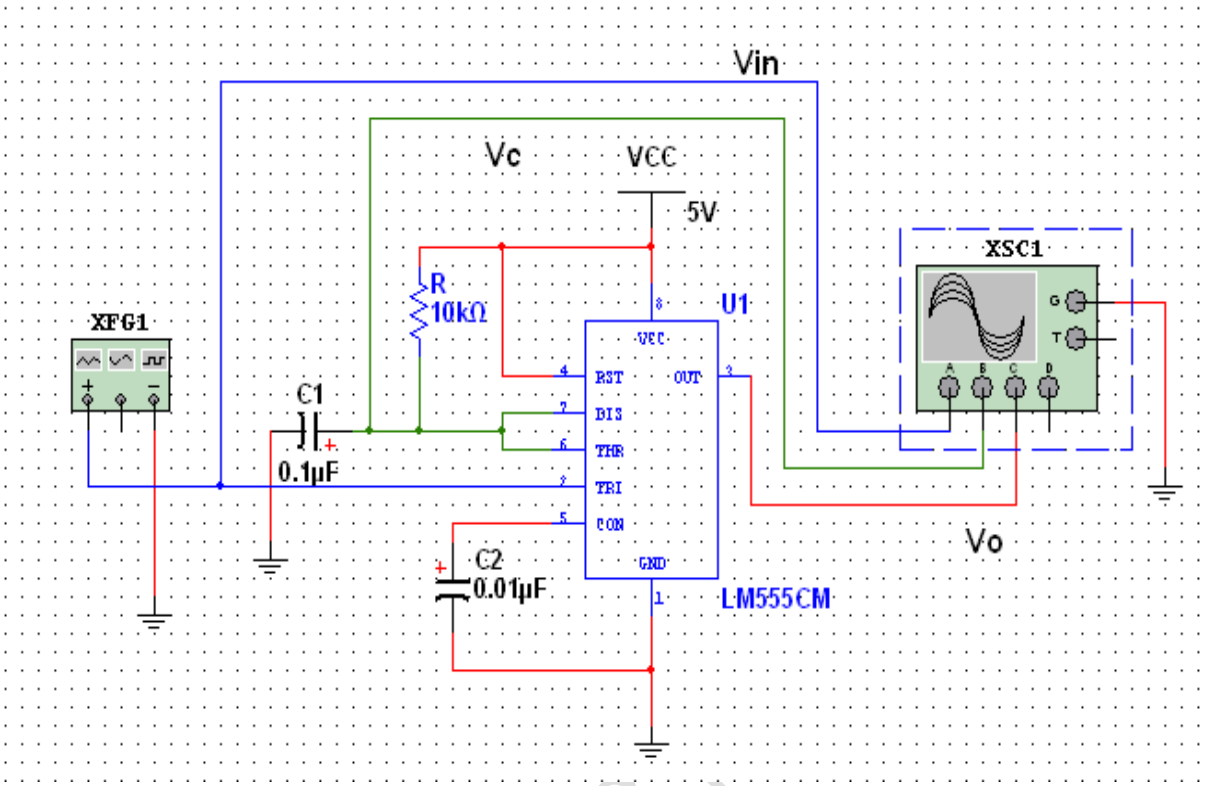

Fig 8.1 Design of mono-stable multi-vibrator using 555-Timer.

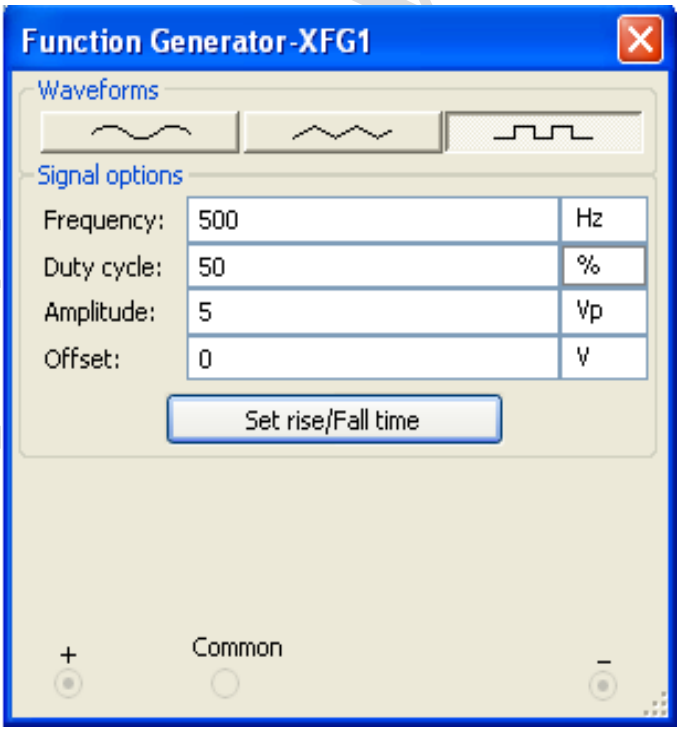

Fig 8.2 Design specifications for monostable multi-vibrator using 555-Timer.

EXPERIMENT-8

Mono-stable Multi-vibrator using IC 555

AIM: Design a mono-stablemulti-vibrator using 555 Timer to produce a pulse width of 1ms.

8.1 APPARATUS:

1. 555 Timer
2. RPS
3. Function generator
4. CRO
5. Resistors
6. Capacitors
7. Bread board

8.2 THEORY:

A switching circuit with one stable output statealso referred to as a one-shot. The one-shot produces a signal output pulse when it receives a valid input trigger signal. This circuit is a mono-stablemulti-vibrator, or one-shot, made with a 555 timer chip. Click the logic input on the left (the "H"), and the output goes high for a short time, and then it goeslow again.A timing interval starts when the trigger input ("tr") is brought low.

When this happens, the555 output goes high. This causes the capacitor to be charged until it reaches 6.67V. Then,the timing interval ends, the output goes low, and the capacitor is discharged through the"dis"input.The capacitor in front of the trigger input causes the mono-stable to be negative-edgetriggered. If the capacitor is replaced with a wire, and the logic input is held low too long,then the 555's output will start to oscillate

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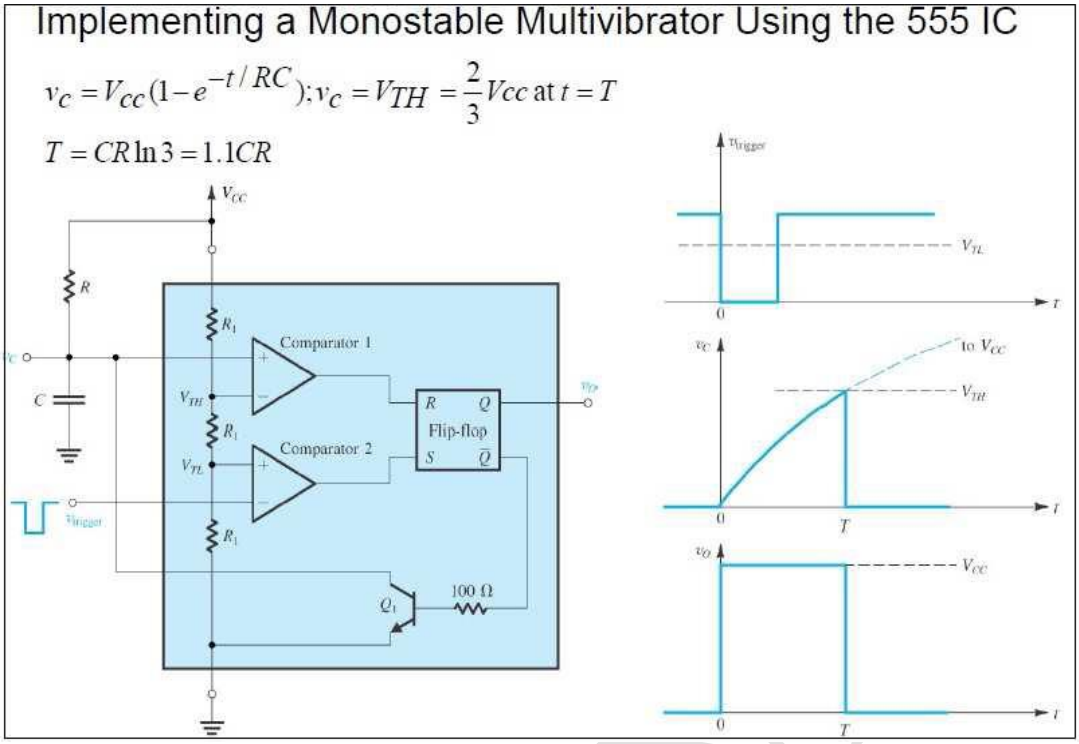

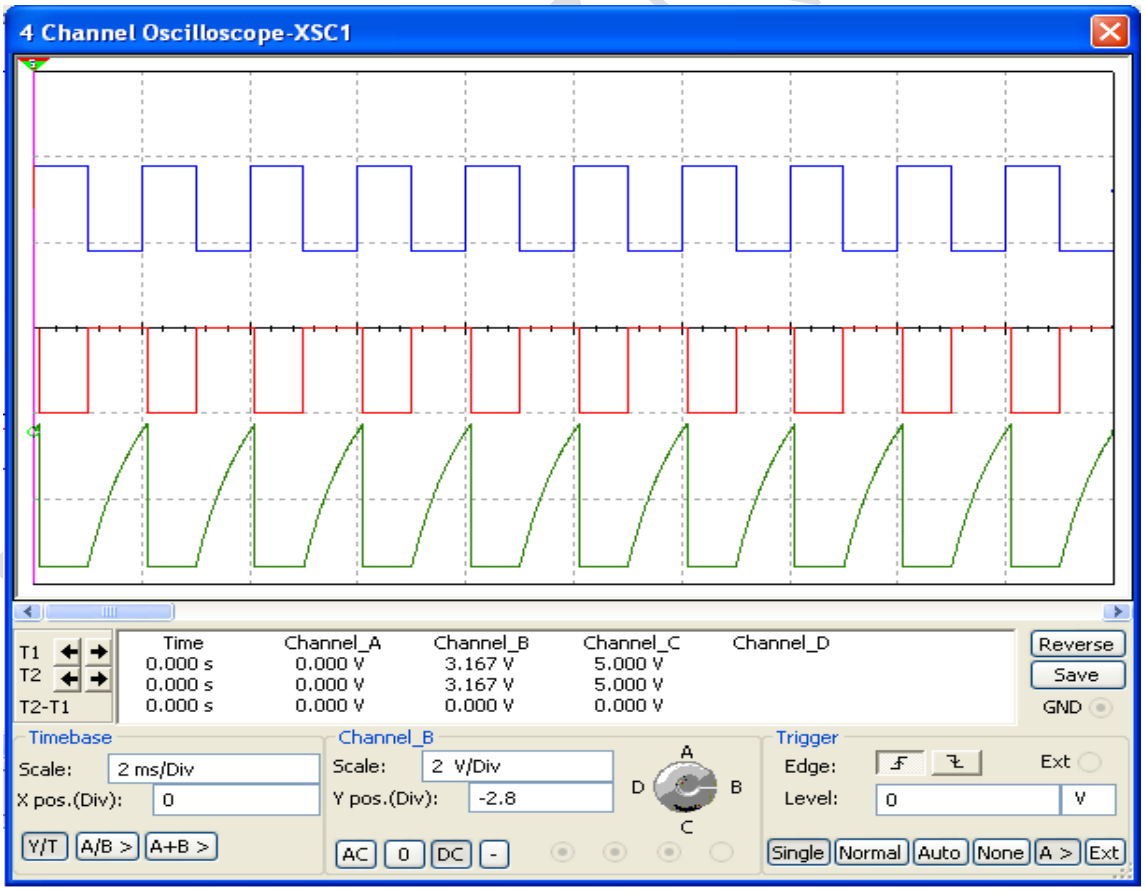

Fig 8.3 Output waveform of monostable multi-vibrator using 555-Timer.

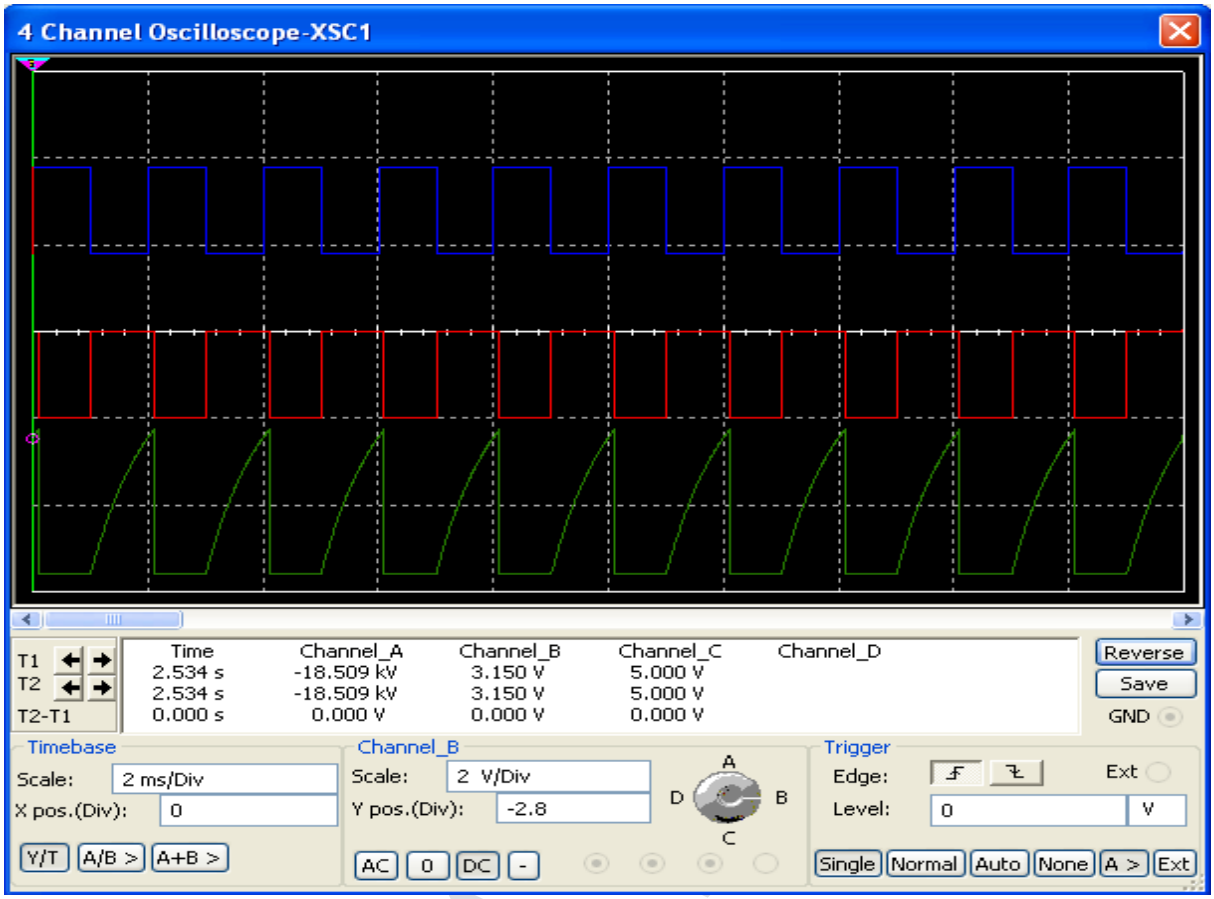

Fig 8.4 Output waveform of monostable multi-vibrator using 555-Timer

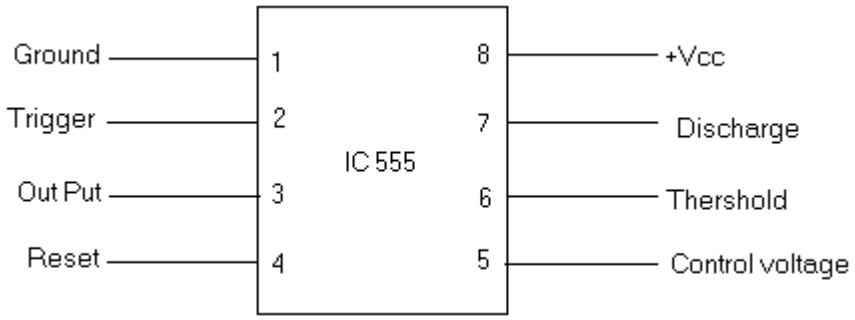

Fig 8.5 pin diagram of IC-555-timer.

8.3 DESIGN EQUATION:

Given that T = 1msec

We know that T=1.1RC

Select R= 10 KΩ, find C= $\frac{T}{1.1R}$ = 0.1 µF

8.4 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Apply trigger input with amplitude of 5V and frequency of 1 KHz and observe the output waveform.
3. Find the voltage across the capacitor and calculate its pulse width from its output waveform.
4. Finally draw the graph for input and output waveforms.

8.5 CALCULATIONS:

1. **Theoretical calculations:**

   $V_0 = V_{cc} = 5V$

   $V_C = \frac{2}{3} V_{CC} = 3.33$

   Pulse width, T = 1.1RC = 1.1msec

2. **Practical calculations:**

   $V_0 = 5V$

   $V_C = 3.33V$

   T = 0.6 msec

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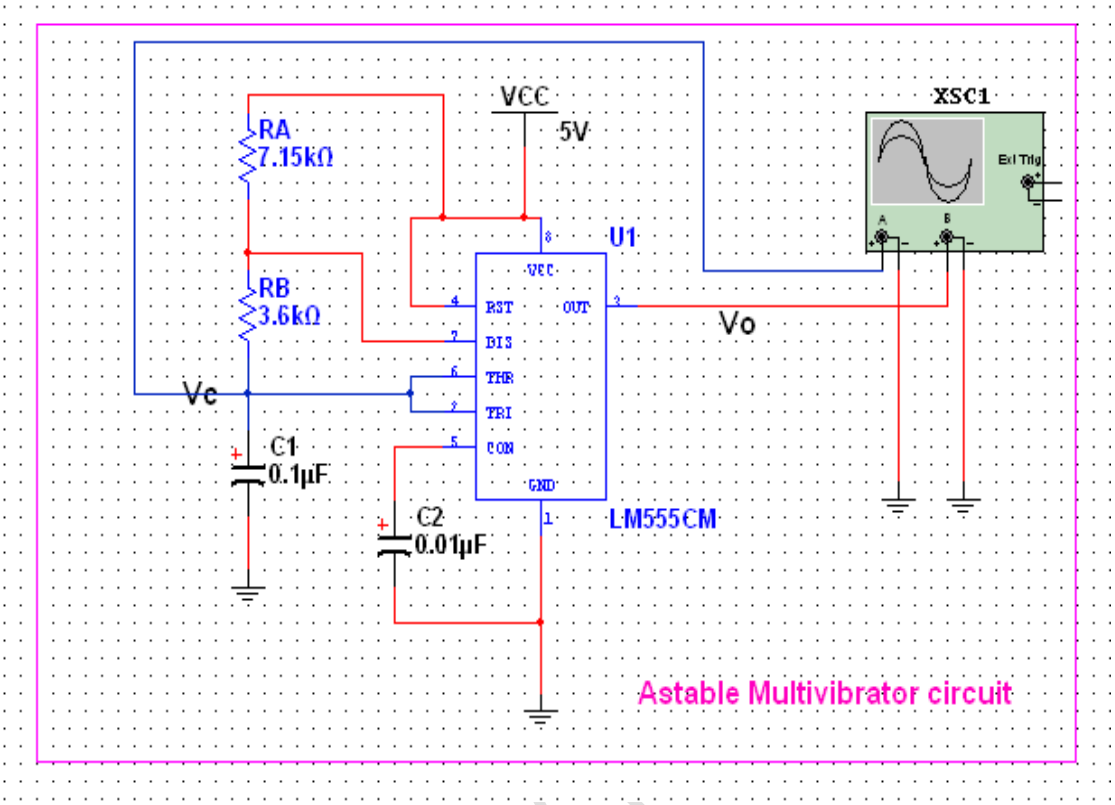

Fig 9.1 Design of Astable multi-vibrator using IC-555-Timer.

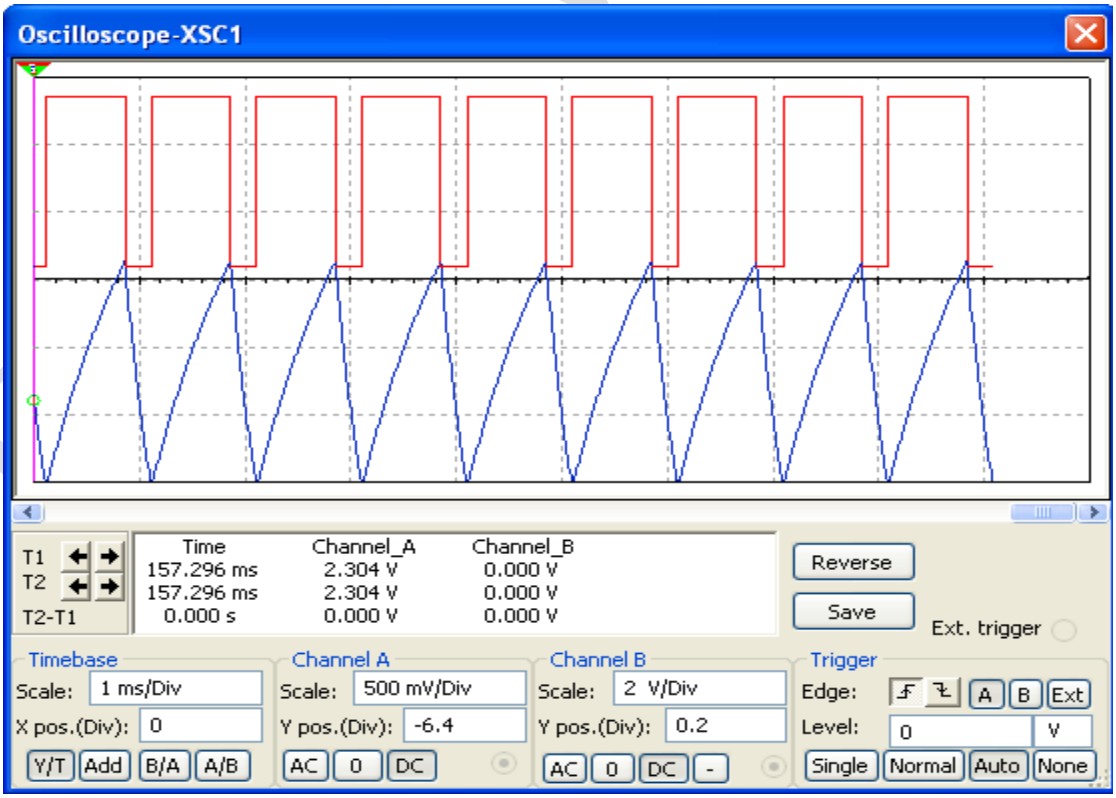

Fig 9.2 Output waveform of Astable multi-vibrator using IC-555-Timer.

EXPERIMENT-9

Astable Multi-vibrator using IC 555

AIM: Design a Astable Multi-vibrator that produces 1KHz unsymmetrical square waveform using 555 timer for duty cycle D = 0.25.

9.1 APPARATUS:

1. 555 Timer
2. RPS
3. CRO
4. Resistors
5. Capacitors
6. Bread board

9.2 DESIGN EQUATIONS:

A switching circuit that has no stable output state,theastable multi-vibrator is a rectangular wave oscillator.Also referred to as a free-running multi-vibrator. The IC555 timer is an 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP –AMP will set the flip-flop. The collector of discharge transistor goes to pin 7.

When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor. When Q is low the transistor opens and the capacitor charges. The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on – off feature is useful in many application.

The lower OP- AMP inverting terminal input is called the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3; the OP-Amp output goes high and resets the flip flop. The output frequency is,

$$f = 1.44/ (RA + RB) C$$

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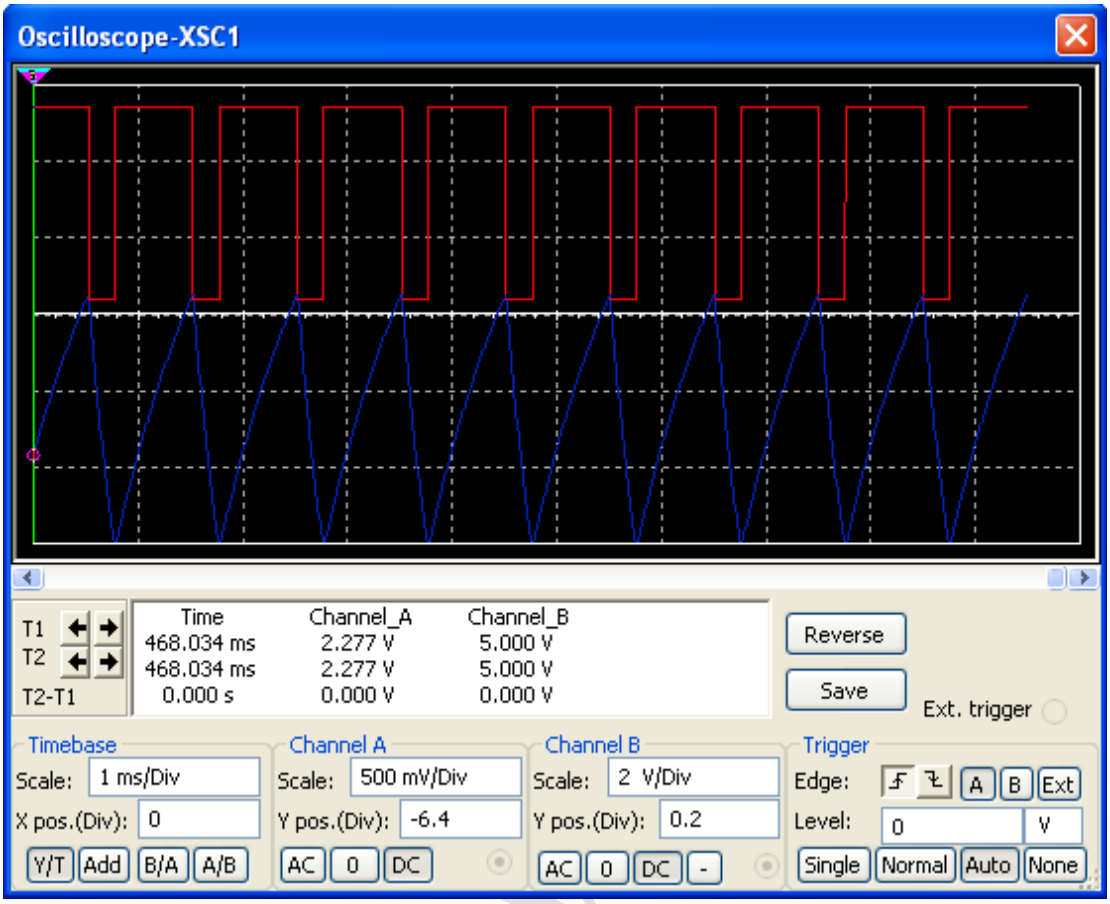

Fig 9.3 Output waveform of Astable multi-vibrator using IC-555-Timer.

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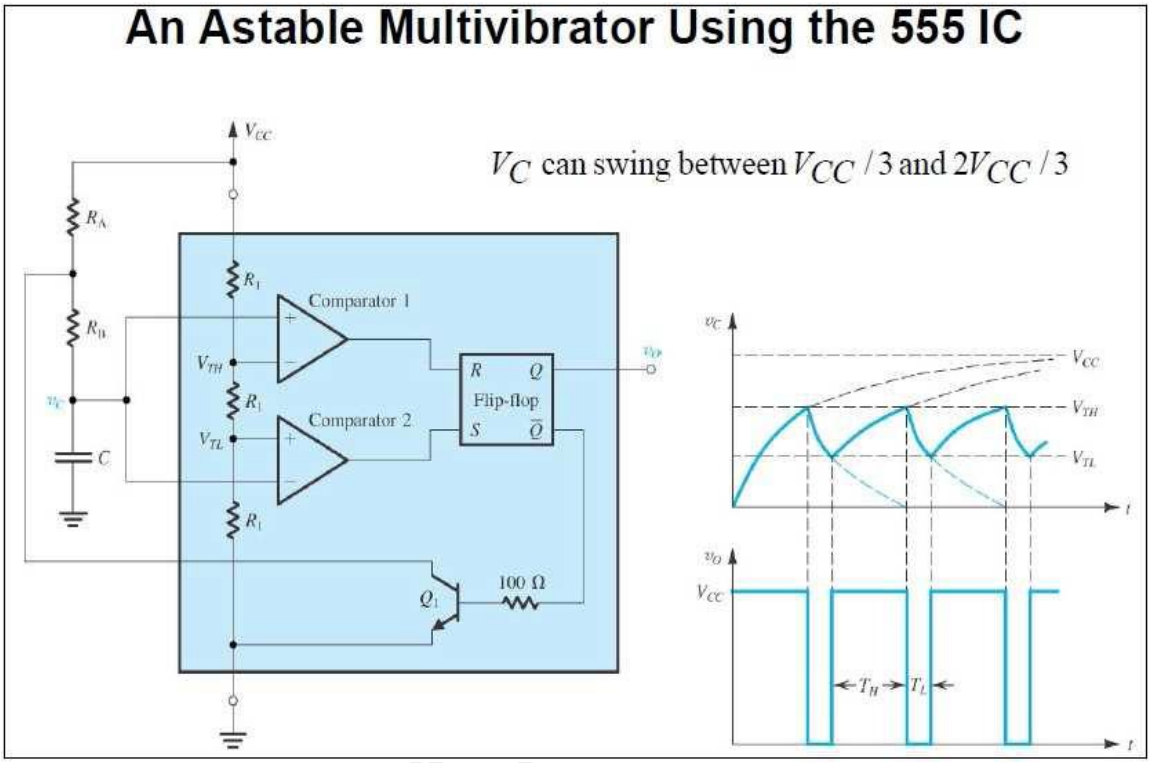
The duty cycle is,

$$D = RB / (RA + 2RB) * 100\%$$

The duty cycle is between 50 to 100% depending on RA and RB



9.3 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Observe the output waveform at pin 3.
3. Find voltage across the capacitor and calculate time period from its output waveform.
4. Now measure duty cycle and then compare it with theoretical value.
5. Draw the graph for input and output waveforms.

9.4 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the OP-AMP before connections.
3. Avoid loose contacts.
4. Avoid errors while observing outputs on CRO.

9.5 CALCULATIONS:

1. Theoretical calculations:

i. $V_0 = V_{cc} = 5V$

ii. $V_C = \frac{1}{3} V_{CC} - \frac{2}{3} V_{CC} = -1.66\ V$

iii. $T_{high} = 0.69(R_A + R_B)C = 0.74\ msec$

iv. $T_{low} = 0.69R_{BC} = 0.249\ msec$

v. Free running frequency (f) = $\frac{1.45}{(R_A + 2R_B)C}$

vi. $D = \frac{R_A}{(R_A + 2R_B)C} = 0.25$

vii. $T = 0.69(R_A + R_B)C = 1\ msec$

2. Practical calculations:

i. $V_0 = 5V$

ii. $V_C = -1.8\ V$

iii. $T_{high} = 0.8\ msec$

iv. $T_{low} = 0.2\ msec$

v. $T = T_{high} + T_{low} = 1\ msec$

vi. $D = \frac{T_{low}}{T} = 0.2$

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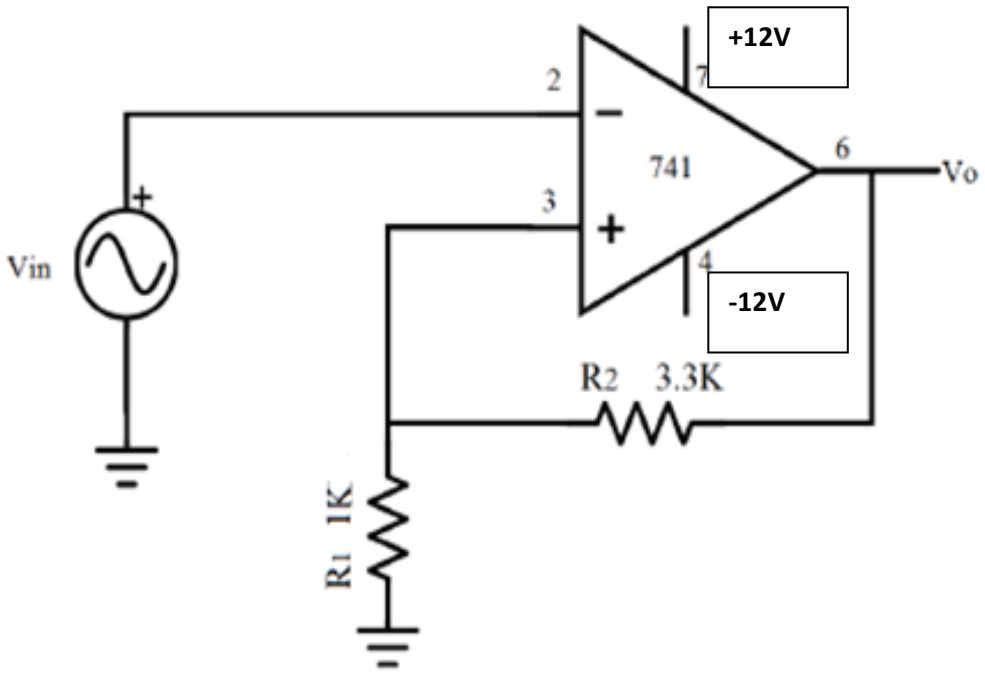

Fig 10.1 Design a Schmitt trigger circuit that takes sinusoidal wave as input and produces square wave output.

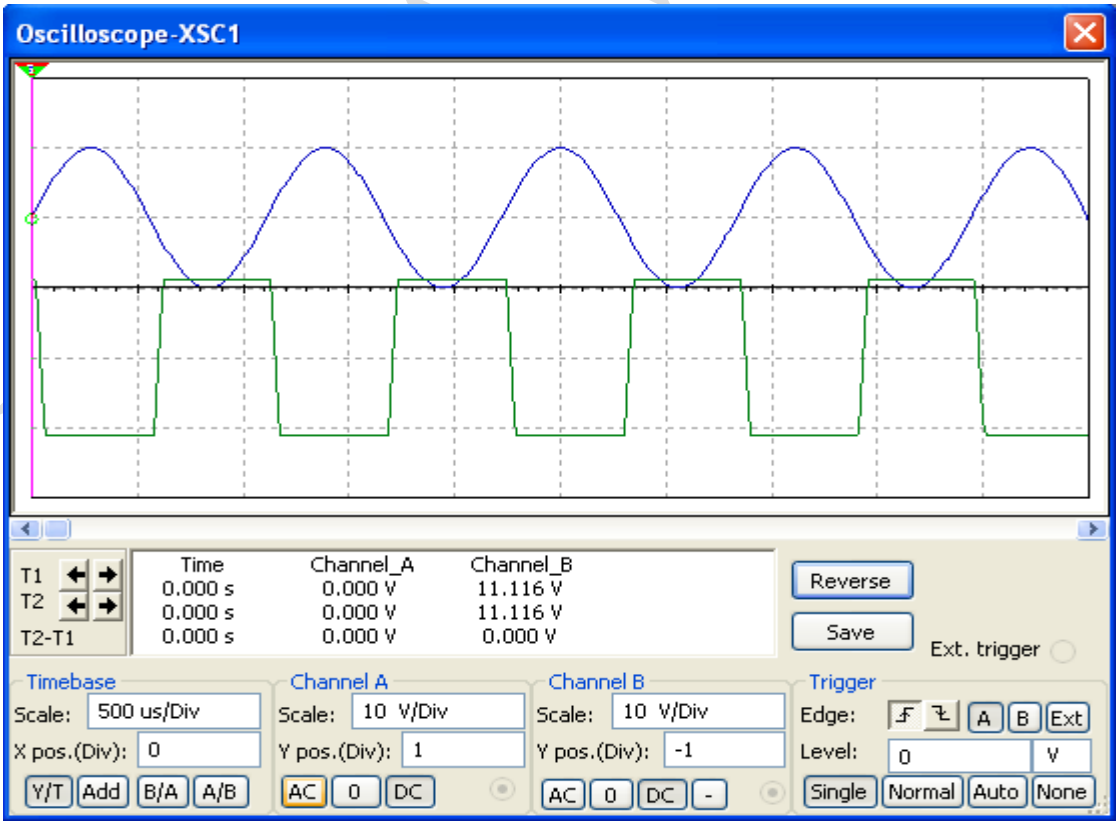

Fig 10.2 Output waveform of Schmitt trigger.

EXPERIMENT-10

SCHMITT TRIGGER CIRCUITS USING IC- 741

AIM: Design a Schmitt trigger circuit that takes sinusoidal wave as input and produces squarewave output and calculate V_{UT} and V_{LT} levels.

10.1 APPARATUS:

1. 555 Timer
2. RPS
3. Function generator
4. CRO
5. Resistors
6. Capacitors
7. Bread board

10.2 PROCEDURE:

1. Design the circuit as per the given specifications and then all the connections are made as per the circuit diagram.
2. Apply V_1 sine wave of sufficient amplitude ($>\frac{V_{CC}}{6} = \frac{2}{3} V_{CC} - \frac{V_{CC}}{2}$) i.e 2.5 V to the circuit.
3. Observe output waveform on CRO and calculate V_{UT} and V_{LT} levels. Now calculate hysteresis and compare it with theoretical value.
4. Observe hysteresis loop on CRO by setting CRO in X-Y mode and measure V_{UT} and V_{LT}.
5. Draw graph for output waveform and Hysteresis loop.

10.3 DESIGN EQUATIONS:

Given that, $V_{UT} = 1V$ and $V_{LT} = -1V$

We know that, $V_{UT} = \frac{R_2}{(R_1 + R_2)} (V_{Sat})$

$V_{UT} = \frac{R_2}{(R_1 + R_2)} (-V_{Sat})$

Select $R_2 = 1K\Omega$, find $R_1 = 11K\Omega$

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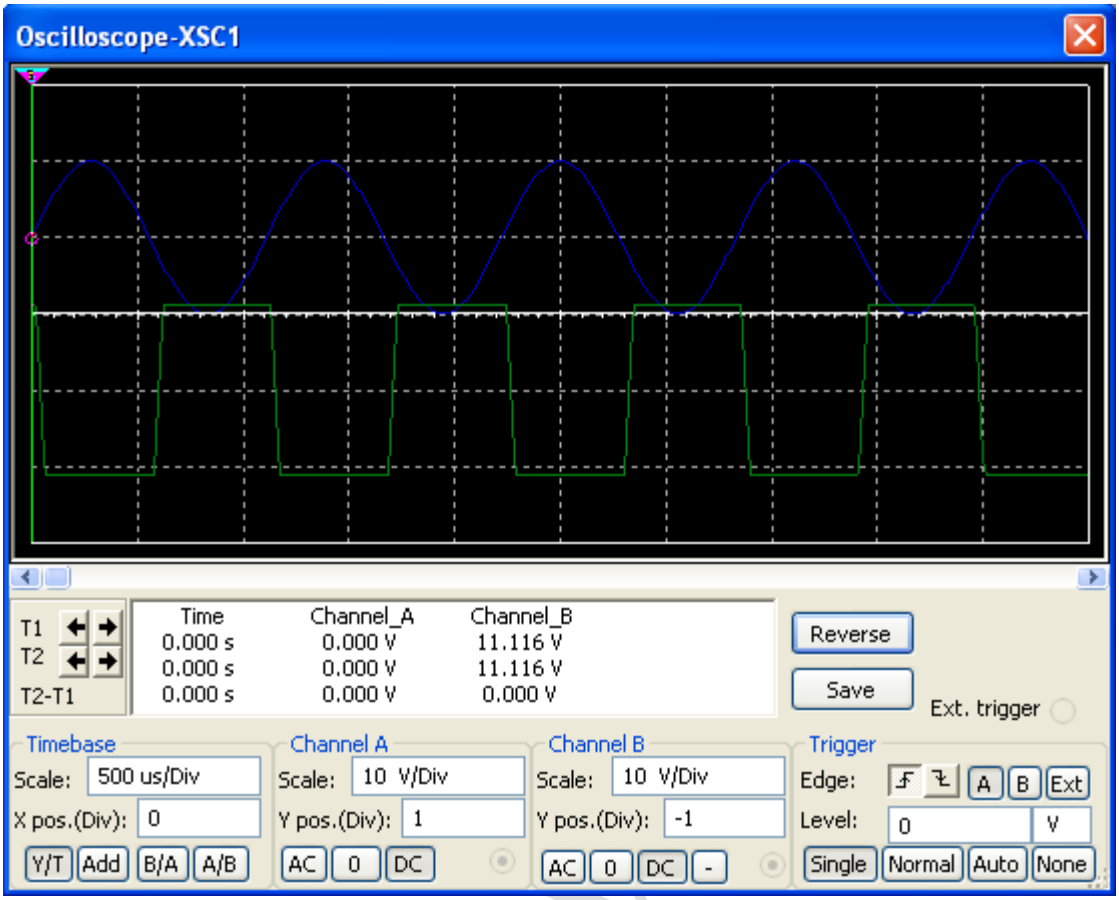


Fig 10.3 Output waveform of Schmitt trigger.

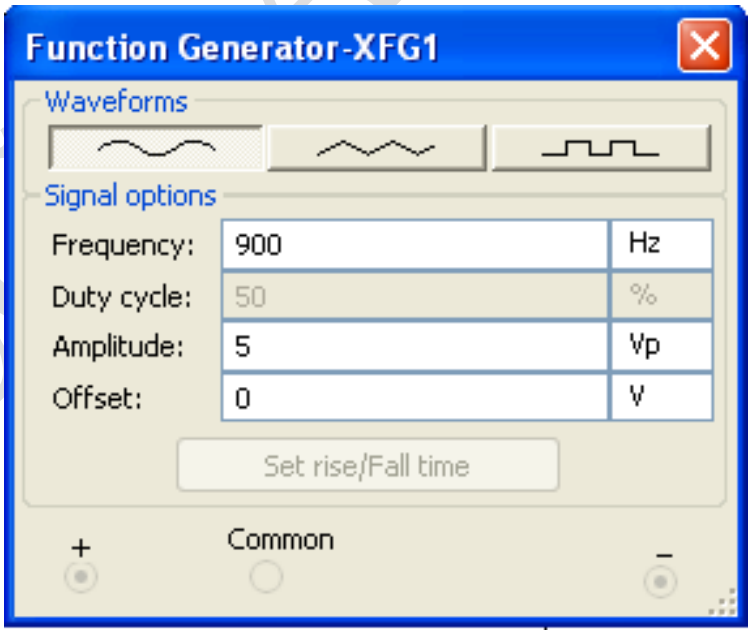


Fig 10.4 Design specifications for Schmitt trigger circuit.

10.4 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the OP-AMP before connections.
3. Avoid loose contacts.
4. Avoid errors while observing outputs on CRO.

10.5 CALCULATIONS:

1. Theoretical calculations:

i. $V_0 = V_{cc} = 5V$

ii. Hysteresis = $V_{UT} - V_{LT} = \frac{2}{3} V_{CC} - \frac{V_{CC}}{3} = \frac{1}{3}(5) = 1.66$ V

2. Practical calculations:

i. $V_0 = V_{cc} = 5V$

ii. Hysteresis = $V_{UT} - V_{LT} = 2V$

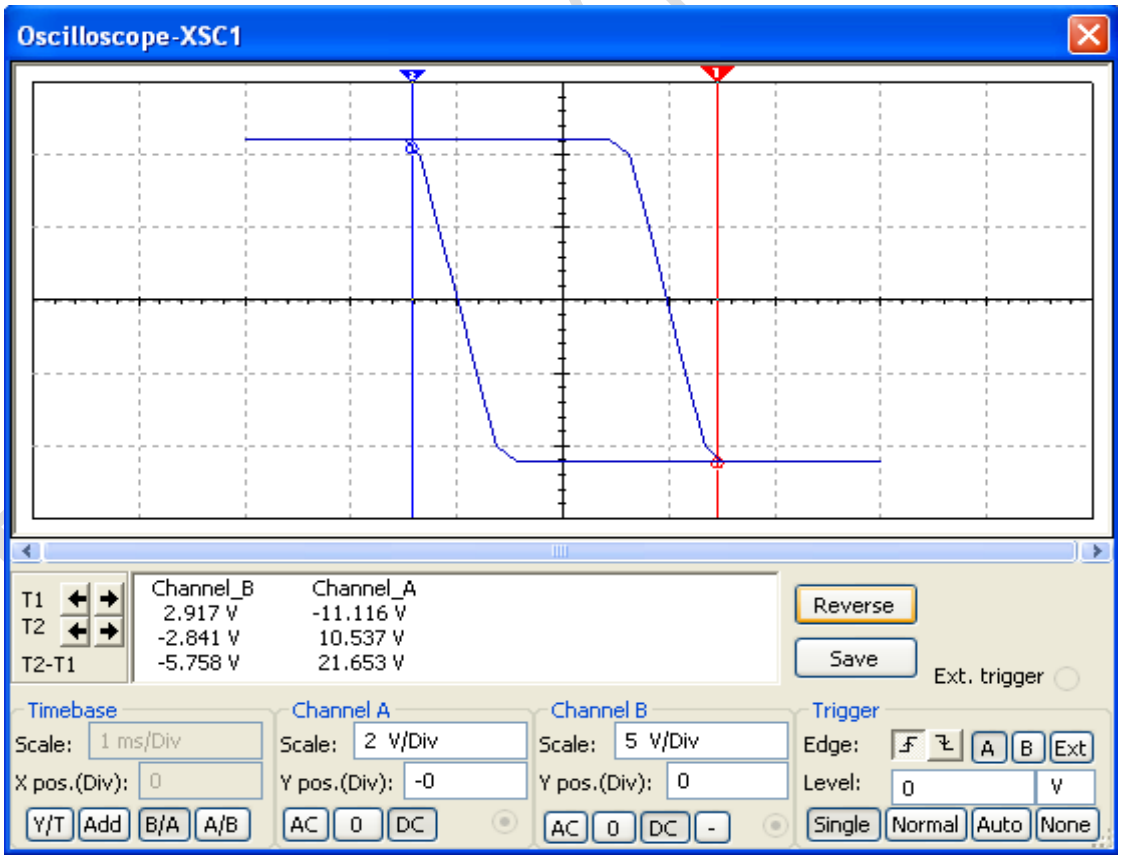


Fig 10.5 V_o versus V_{in} Plot of the Hysteresis voltage.

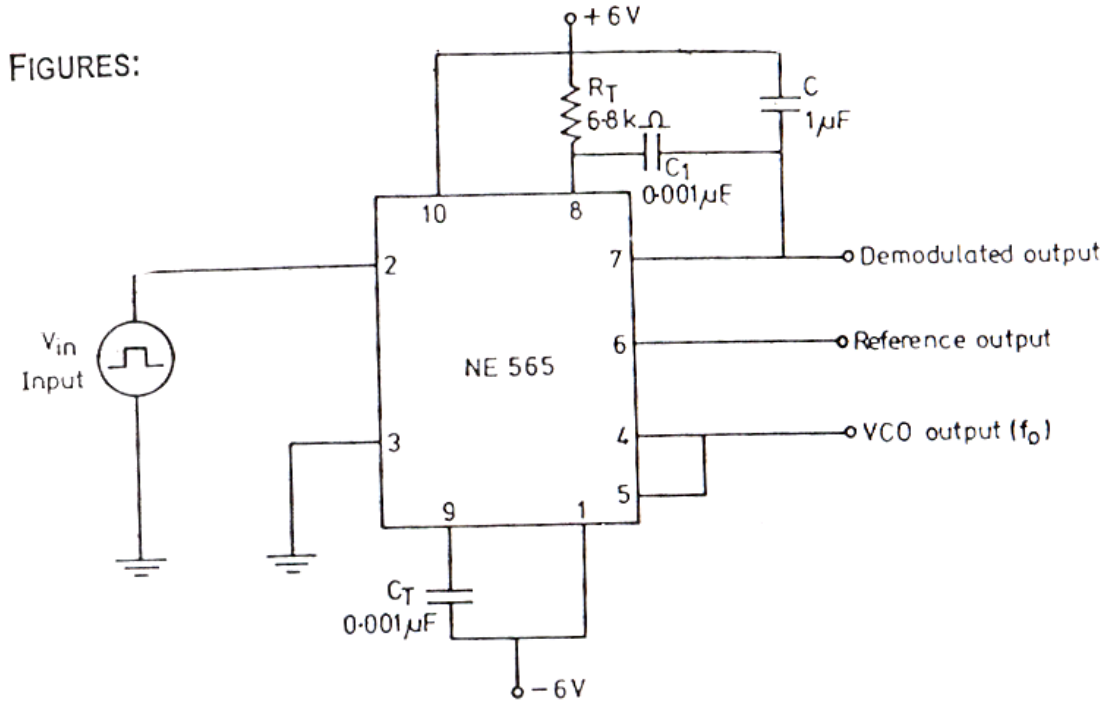
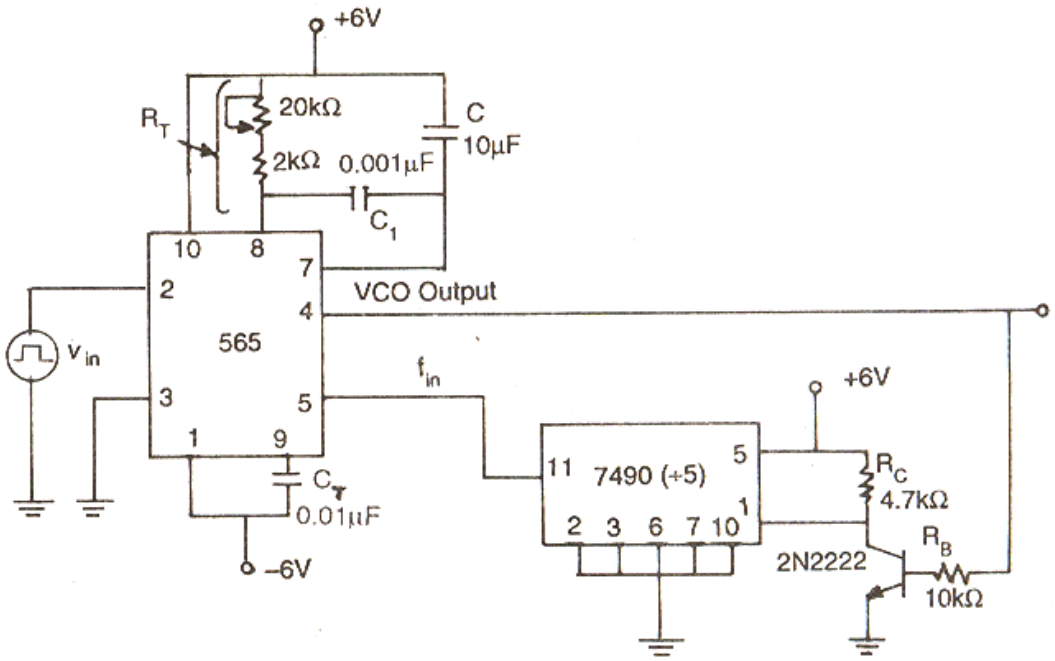


Fig 11.1 Circuit diagram.



EXPERIMENT-11

IC-565 PLL APPLICATIONS

AIM: To study the operation of NE565 PLL.

11.1 APPARATUS:

1. DC power supply
2. IC-565
3. CRO
4. Function generator
5. Resistors
6. Capacitors
7. Bread board

11.2 THEORY:

PHASE LOCKED LOOP OPERATION:

The basic concept of the operation of the PLL is relatively simple, although the mathematicalanalysis and many elements of its operation can become more complicatedThe Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters thephase detector. Here the phase of the signals from the VCO and the incoming reference signalare compared and a resulting difference or error voltage is produced. This corresponds to thephase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs manyof the properties of the loop and removes any high frequency elements on the signal. Oncethrough the filter the error signal is applied to the control terminal of the VCO as its tuningvoltage. The sense of any change in this voltage is such that it tries to reduce the phasedifference and hence the frequency between the two signals. Initially the loop will be out oflock, and the error voltage will pull the frequency of the VCO towards that of the reference,until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. Byusing an amplifier between the phase detector and the VCO, the actual error between

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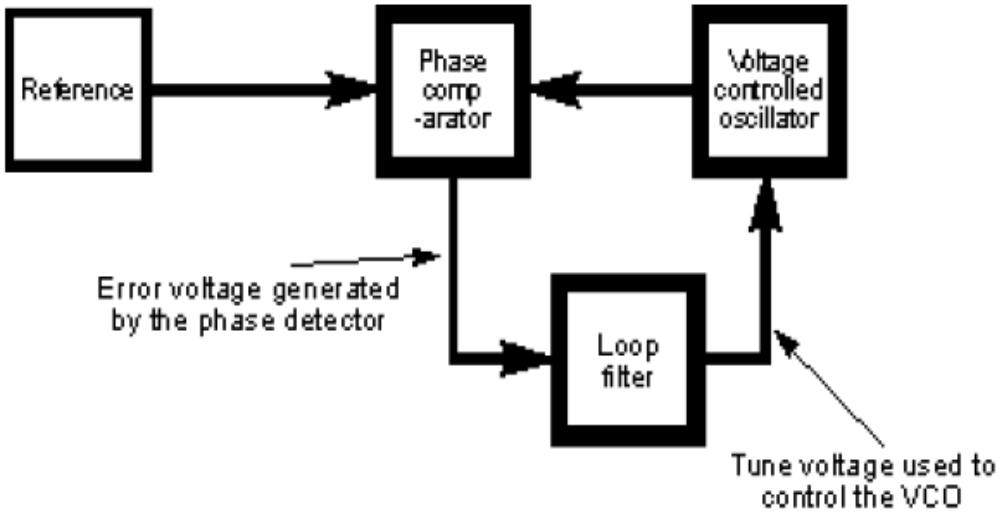
thesignals can be reduced to very small levels. However some voltage must always be present atthe control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between thereference signal and the VCO is not changing. As the phase between these two signals is notchanging means that the two signals are on exactly the same frequency.The 565 is available as a 14-pin DIP package. It is produced by Signetics Corporation. TheoutputFrequency of the VCO can be rewritten as:

$$Fo= (0.25/Rt\ Ct)\ Hz$$

Where RT and CT are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 KΩ and 20 KΩ is recommended for RT. The VCO free running frequency isadjusted with RT and CT to be at the centreof the input frequency range.



Block diagram of a basic phase locked loop (PLL)

11.3 PROCEDURE:

1. Connect the circuit using the component values as shown in the figure
2. Measure the free running frequency of VCO at pin 4 with the input signal Vin set zero. Compare it with the calculated value = 0.25/ RTCT
3. Now apply the input signal of 1Vpp square wave at a 1kHz to pin 2
4. Connect 1 channel of the scope to pin 2 and display this signal on the scope
5. Gradually increase the input frequency till the PLL is locked to the input frequency.This frequency f1gives the lower ends of the capture range. Go on increase the inputfrequency, till PLL tracks the input signal, say to a frequency f2. This frequency f2gives the upper end of the lock range. If the input frequency is increased further theloop will get unlocked.
6. Now gradually decrease the input frequency till the PLL is again locked. This is thefrequency f3, the upper end of the capture range. Keep on decreasing the inputfrequency until the loop is unlocked. This frequency f4 gives the lower end of the lockrange
7. The lock range ΔfL = (f2 – f4) compare it with the calculated value of (±7.8fo/12)Also the capture range is Δfc = (f3 – f1). Compare it with the calculated value ofcapture range.Δfc = ± (ΔfL/(2_)(3.6)(103)Xc)1/2
8. To use PLL as a multiplie5r, make connections as show in fig. The circuit uses a 4-bitbinary counter 7490 used as a divide-by-5 circuit.
9. Set the input signal at 1Vpp square wave at 500Hz
10. Vary the VCO frequency by adjusting the 20KΩ potentiometer till the PLL is locked.Measure the output frequency
11. Repeat step 9 and 10 for input frequency of 1 kHz and 1.5 kHz.

11.4 OBSERVATIONS:

1. fo = _____
2. f_L = _____
3. f_C = _____

11.5 CALCULATIONS:

1. Δf_L = (f2 – f4) = (±7.8fo/12)

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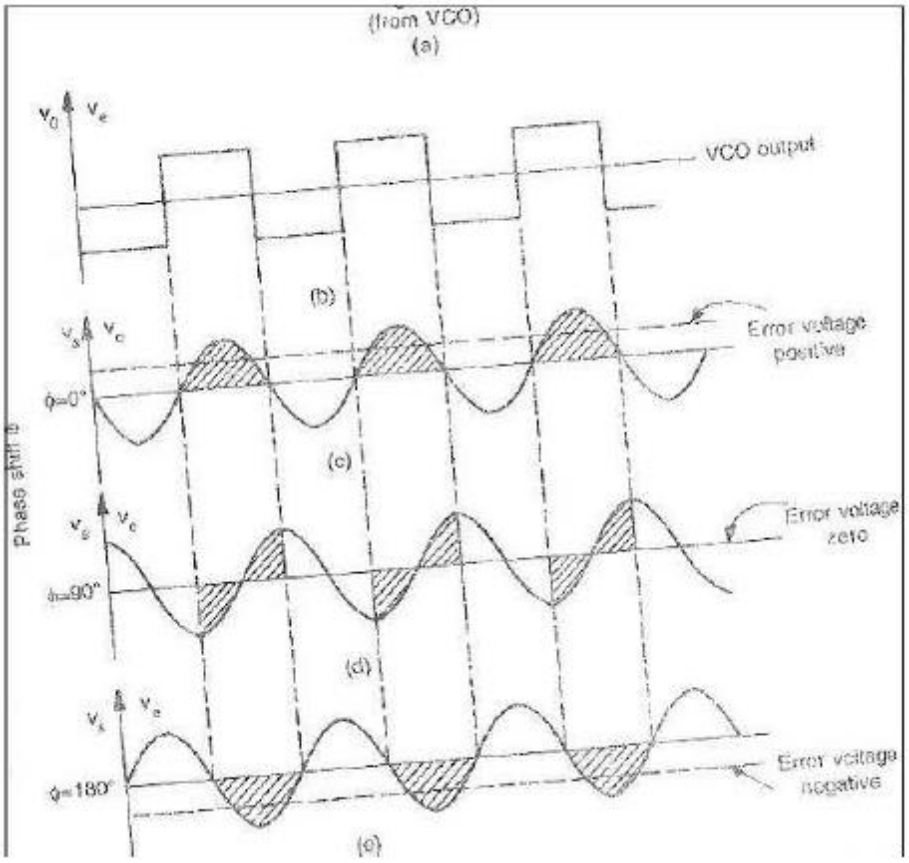
2. $\Delta f_C = \pm (\Delta fL/(2\_)(3.6)(103)Xc)1/2$

11.6 RESULT:

1. fo = _____
2. f_L = _____
3. f_C = _____

11.7 GRAPH:



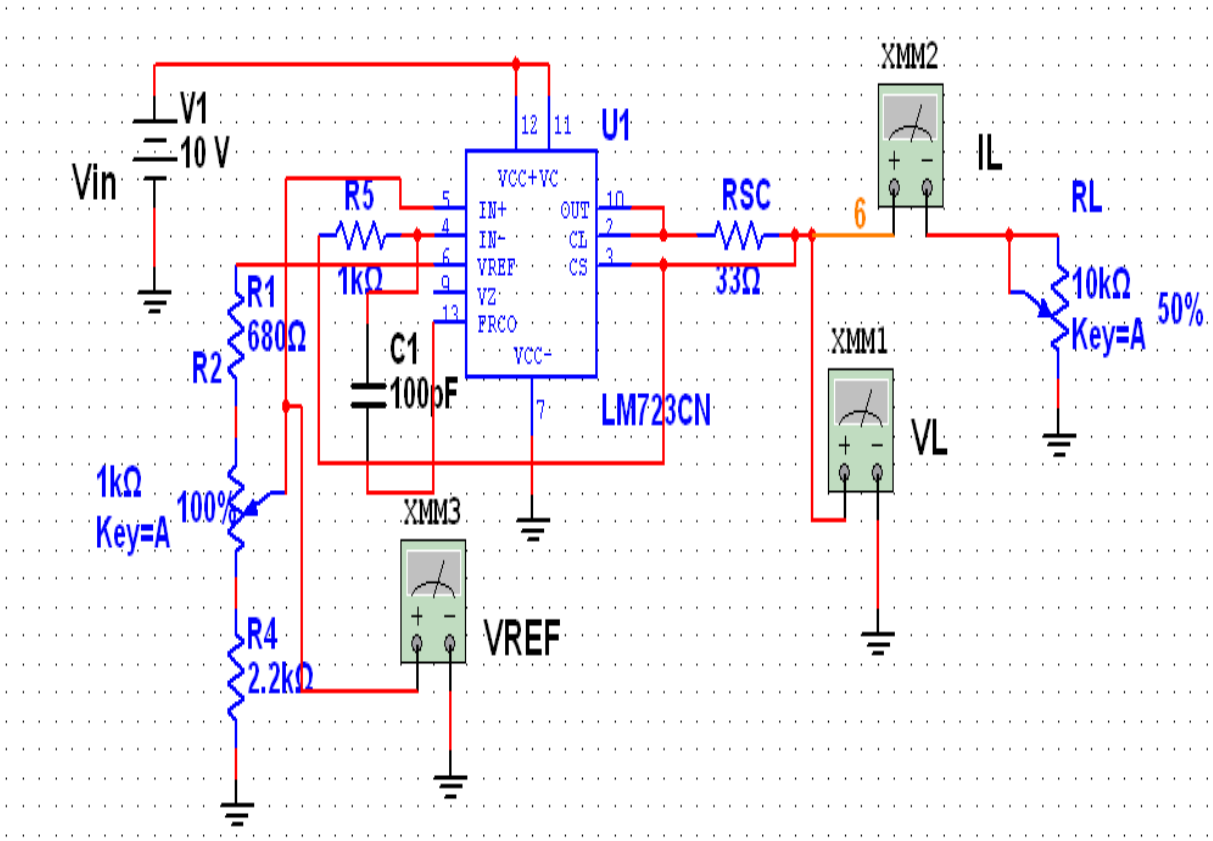


Fig 12.1 IC-723 General purpose voltage regulator.

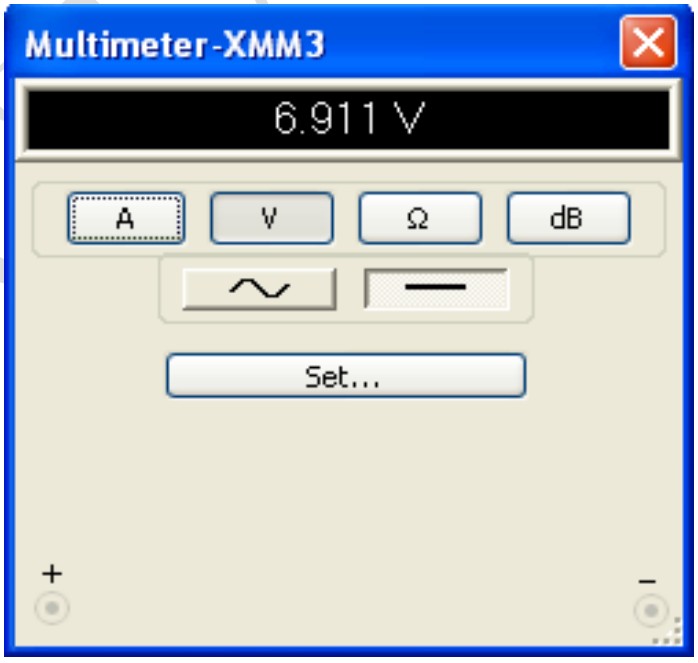


Fig 12.2 V_{ref} with respect to ground when load is removed.

EXPERIMENT-12

VOLTAGE REGULATOR USING IC-723

AIM: To observe the regulation parameters such as line and load of voltage regulator.

12.1 APPARATUS:

1. Three terminal voltage regulators-7805, 7809, 7912
2. RPS
3. Bread board
4. Connecting wires
5. IC-723
6. Resistors
7. Capacitors

12.2 THEORY:

The IC723 is a general purpose regulator which can be adjusted over a wide range of both +ve or –ve regulated voltage. This is a 14-pin DIP package. . This IC is inherently low current device but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short-circuit current limits. The IC723 has two sections. The first section consists of Zener Diode constant current source and a reference amplifier. The other section of the IC consists of an error amplifier series pass transistor and a current limit transistor. This is a 14-pin DIP package. The main features of 723 include an input voltage of 40v max, output voltage is adjustable from 2V to 37V, 150mA output current without external pass resistor, can be used as either a linear or a switching regulator.

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V_{in}(in Volts)	V_{out}(in Volts)
1	394.729m
2	649.806m
3	1.169
4	1.803
5	2.44
6	3.09
7	3.738
10	4.823
15	4.824
20	4.824
25	4.824
30	4.824

Fig 12.3 Line Regulation for fixed 5VVoltage regulator IC-723

R_L(in KΩ), V_{in}=constant=10V	V_{out}(in Volts)
1	4.823
2	4.823
3	4.823
4	4.823
5	4.823
6	4.823
7	4.823
8	4.823
9	4.823
10	4.823

Fig 12.4 Load Regulation for IC-723

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12.3 Procedure:

1. Connect the 723 regulator as shown in the circuit diagram.
2. Set Dc power supply voltage V_{in} to +10V measure and record $V_{ref}$with respect toground. With load R_L(10kΩ pot) removed from the circuit (output open). Measurethe minimum and maximum output voltage by rotating the 1kΩ pot through itsfull range.
3. Now adjust the 1kΩ pot so that $V_o$is +5V dc. Measure the voltage between thewiper arm of the 1 kΩ pot and ground.
4. Adjust the load R_L (10 kΩ) pot until the load current I_L = 1 mA. Record V_L.Repeat for different values of load currents 5mA, 10mA, 15mA, 18mA. Calculatethe load regulation and compare with manufacturer's specifications
5. Gradually increase the load current above 18mA, you will see that the loadvoltage suddenly decreases when the load current is about 18 to 20 mA. Now thevoltage across R_{SC} is enough to begin current limiting. Measure and record a fewvalues of load current and load voltage below and above the current limiting point.Plot a graph of V_L Vs I_L from the data obtained in steps 4 and 5.

12.3 PRECAUTIONS:

1. Check the circuit connections before switching on the power supply.

2. Check the connections between pin no.2 and ground.

3. Check the continuity of the connecting wires.

12.4 OBSERVATIONS:

1. The load regulation
2. The line regulation

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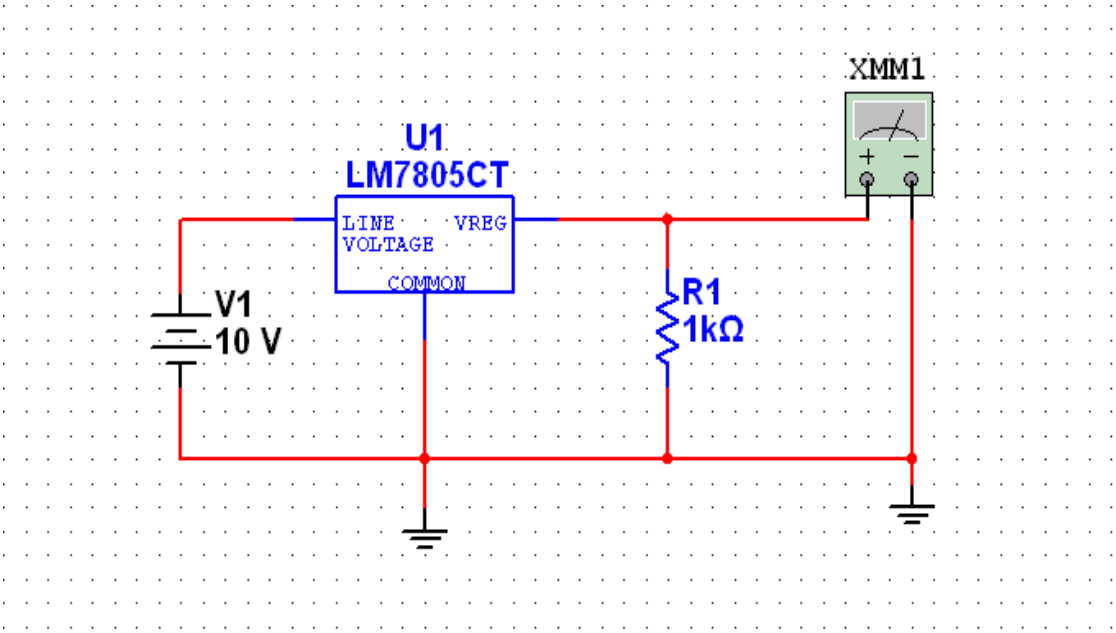

Fig 13.1 5vFixed Voltage regulator 7805.

V_{in}, R_L=constant= 1KΩ	V_{out}
1	194.79n
2	591.92n
3	1.561
4	2.54
5	3.51
6	4.48
7	5.001
10	5.002
15	5.003
20	5.004
25	5.005

Fig 13.2 Line Regulation for fixed 5V Voltage regulator 7805.

EXPERIMENT-13

Three Terminal Voltage Regulators –7805, 7809, 7912

AIM: To observe the regulation parameters such as line and load of voltage regulator IC7805, IC 7809, and IC7912.

13.1 APPARATUS:

1. IC 7805
2. IC 7809
3. IC 7912
4. Resistors
5. Voltmeters
6. Power Supply
7. Bread Board

13.2 Theory:

78xx series are three terminal positive fixed voltage regulators. There are sevenoutput voltage options such as 5, 6, 8, 12, 15, 18 and 24V. In 78XX the last twonumbers indicate the output voltage. Thus 7805 represents a 5V generator. Theseare also available in 79XX series of fixed output, negative are also available in79XX which are complement to the 78XX series device. There are fourcharacteristics of three terminal IC regulators.

V0: The regulated output voltage is fixed at a value as specified by manufacture.eg. 78XX has output voltage at 5, 6, 8, …..etc.

Vin >=1*Volt* +2*Volts* : The unregulated output voltage must be at least 2V morethan the regulated output voltage.

I0 (Max): The load current may vary from 0 to rated maximum output current.The IC is usually provided with a heat sink.

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Thermal Shut down: The IC has a temperature sensor which turns off the ICwhen it becomes too hot. The output current will drop and remain there until theIC has cooled significantly.

Line Input Regulation : It is defined as percentage change in the output voltagefor a change in the input voltage

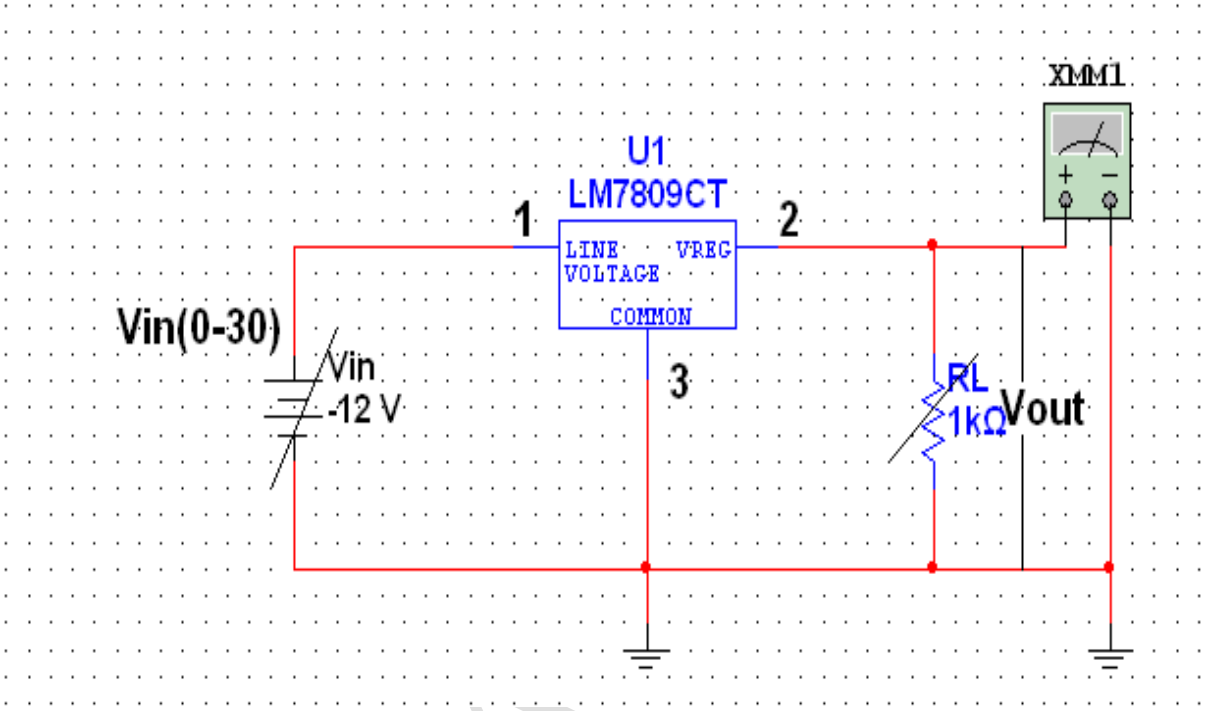

Fig 13.3 9Vv Fixed Voltage regulator 7809.

V_{in}(Volts)	V_{out}(Volts)
1	0.00
2	0.00
3	1.62
4	3.43
5	4.42
7	6.46
8	7.40
9	8.45
10	8.97
15	8.99
20	8.99

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Fig 13.4 Line Regulation for fixed9VVoltage regulator 7809.

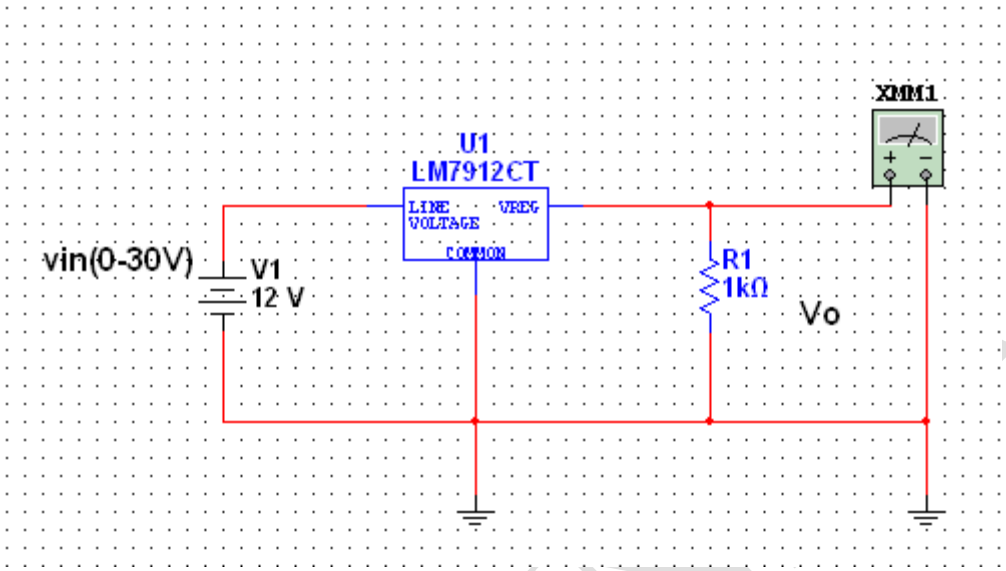

Fig 13.5 -12v Fixed Voltage regulator IC-7912.

V_{in}(Volts)	V_{out}(Volts)
-1	-0.00
-2	-0.00
-3	-0.01
-4	-2.85
-5	-3.77
-6	-4.71
-7	-6.62
-8	-7.66
-9	-8.66
-10	-9.58
-11	-10.54
-12	-11.52
-13	-12.00
-14	-12.00
-15	-12.00

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Fig 13.6 Line Regulation for fixed -12VVoltage regulator IC-7912.

13.3 PROCEDURE:

a. Line Regulation:

1. All the connections are made as per the circuit diagram.
2. Connect the load resistance of any value with higher voltage.
3. Vary the input DC supply in regular steps.
4. Note down the corresponding output voltage using a voltmeter.
5. Plot the graph: V_{in}Vs $V_{0.}$

b. Load Regulation:

1. For the same circuit shown in the fig, fix the DC supply voltage more than regulated value.
2. Replace the fixed resistance by a decade resistance box.
3. Vary the load resistance in regular steps of 1 KΩ.
4. Note down the corresponding output across the load using voltmeter.
5. Plot the graph: R_LVs V_0.

13.4 PRECAUTIONS:

1. Keep current knob of power supply in max position.
2. Check the regulator before connections.
3. Avoid loose contacts.

13.5 OBSERVATIONS:

1. The load regulation
2. The line regulation

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13.6 RESULT:

7805	V_{in}= 7V	7912	V_{in}= 15V	7809	V_{in}= -14
R_L(KΩ)	V_{out}	R_L(KΩ)	V_{out}	R_L(KΩ)	V_{out}
1	4.99	1	-12.00	1	8.97
2	4.99	2	-12.00	2	8.97
3	4.99	3	-12.00	3	8.97
5	4.99	4	-12.00	4	8.97
6	4.99	5	-12.00	5	8.97
10	4.99	6	-12.00	10	8.97

Fig 13.7 Load Regulation for IC-7805, IC-7912, IC-7809

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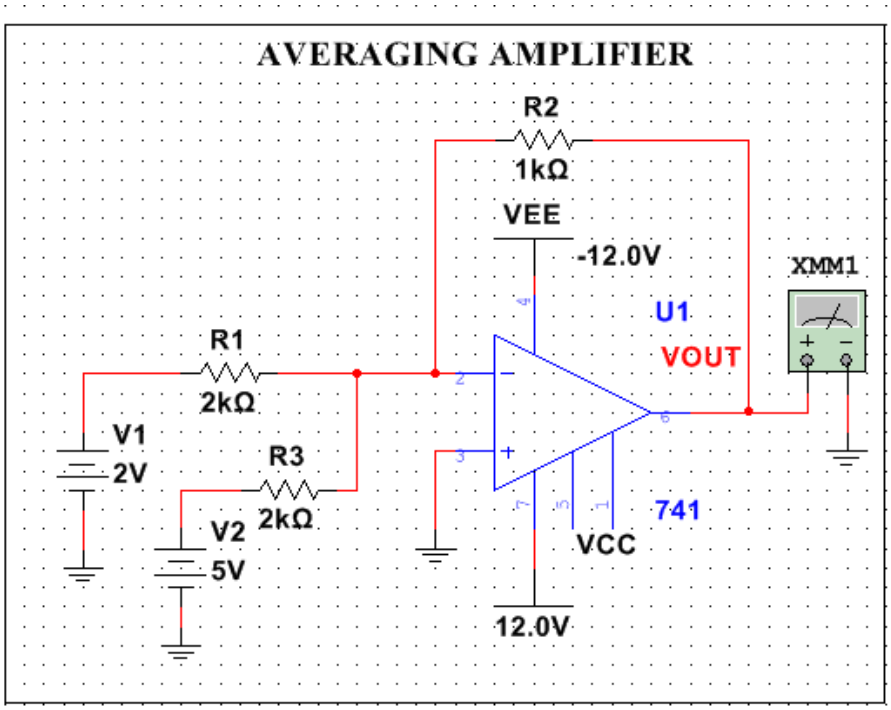
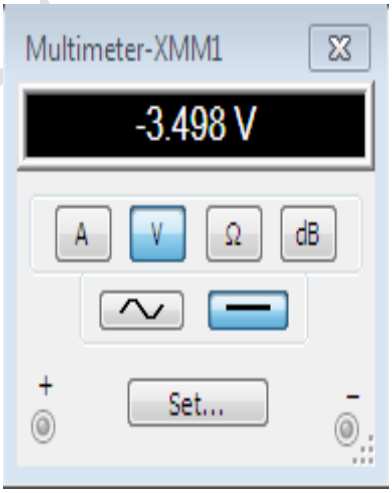


Fig 1.1 Averaging Amplifier



Additional Experiment-1

Averaging amplifier

Aim: Verify the functionality of OP-AMP as average amplifier

1.1 APPARATUS:

2. IC 741
3. Resistors
4. Voltmeters
5. Power Supply
6. Bread Board

1.2. Theory:

Averaging Amplifier

A summing amplifier designed such that the output voltage is equal to the average of all input voltages,is called an average amplifier. The average amplifier (shown in figure 3.4) output can be achieved bymaking a gain (i.e.)$Rf/Rin$of summing amplifier equal to the reciprocal of number of inputs.

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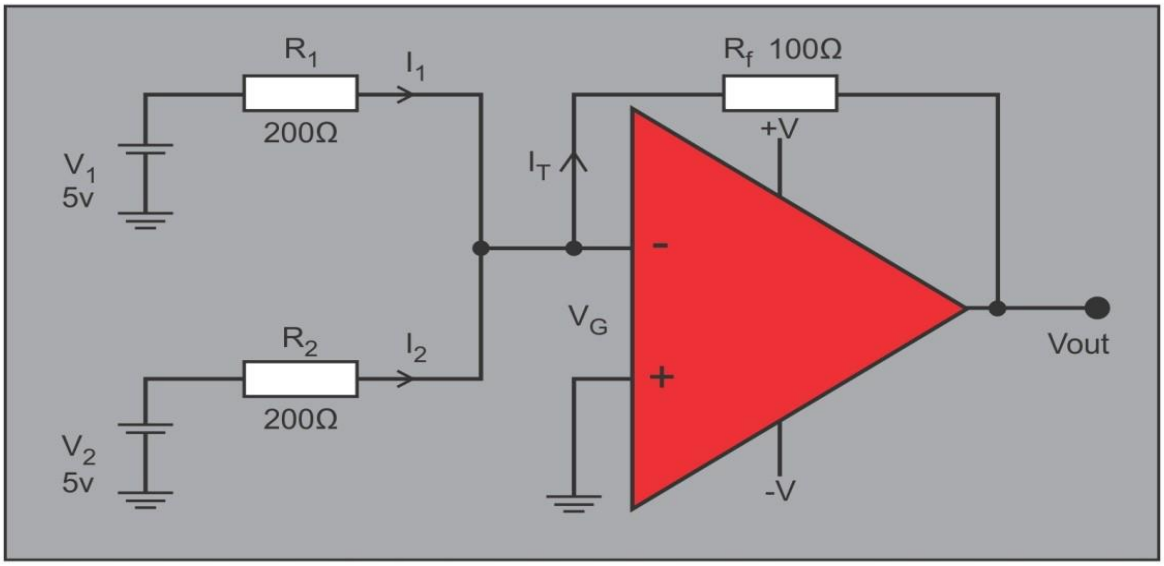

Fig 1.2 Averaging Amplifier

1.3 Design Equations:

$$V_{out} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right) R_f$$

Let $R_1 = R_2 = 200\ \Omega$, $R_f = 100\ \Omega$ and $V_1 = V_2 = 5\ V$

$$V_{out} = -\left(\frac{5}{200} + \frac{5}{200}\right) 100$$

$$V_{out} = -5\ V$$

$$V_{inaverage} = \left(\frac{V_1 + V_2}{2}\right)$$

$$V_{inaverage} = \left(\frac{5+5}{2}\right) = 5V$$

1.4 Procedure:

1. Check the components.

2. Setup the circuit on the breadboard and check the connections.

3. Switch on the power supply.

4. Apply the DC supplies at inverting terminal.

5. Observe the output at multimeter.

1.5 Calculations:

$V_{INAVG} = \frac{(V1+V2)}{2}$

$V_{INAVG} = \frac{2+5}{2} = 3.5\ V$

$$V_{out} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right) R_f$$

$V_{OUT} = -\left(\frac{2}{2K} + \frac{5}{2K}\right) 1K = \frac{7}{2K} X 1K = -3.5\ V$

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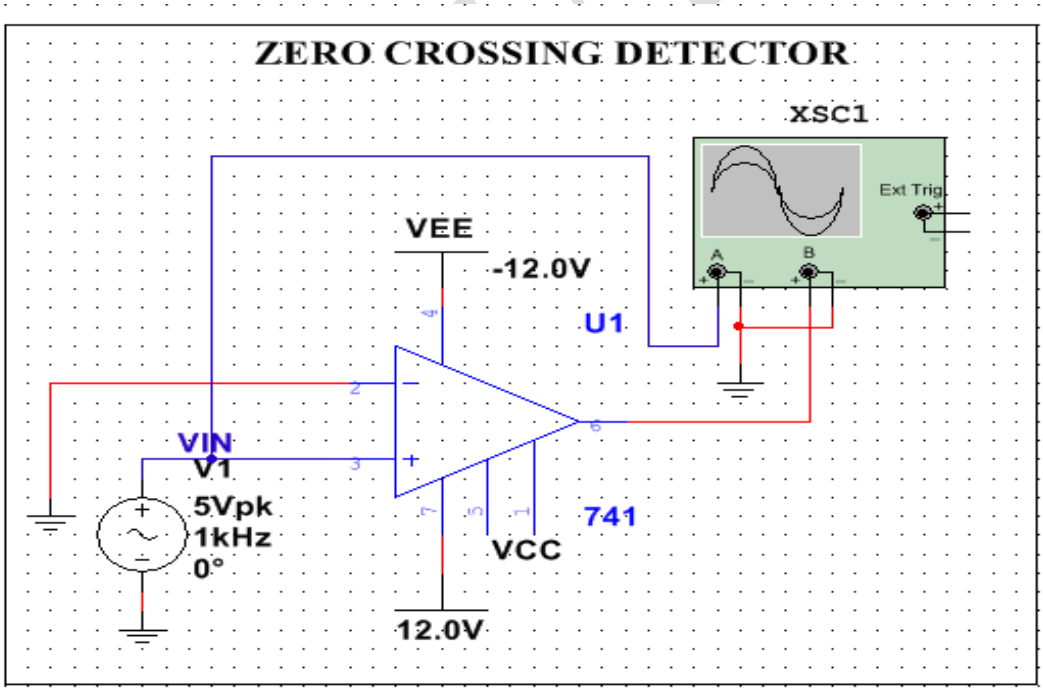
ZERO CROSSING DETECTOR
XSC1
Ext Trig
A
B
VEE
-12.0V
U1
VIN
V1
5Vpk
1kHz
0°
741
VCC
12.0V

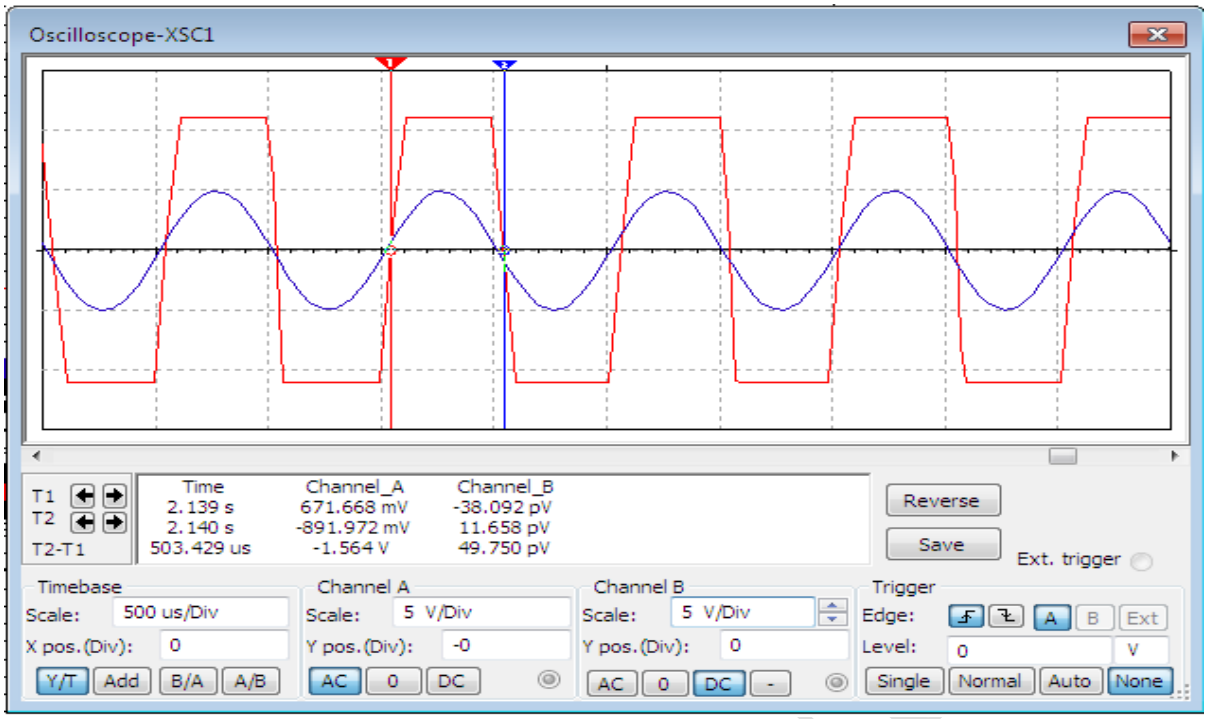

Fig 2.1: Zero crossing points of sinusoidal signal detected by zero crossing detector circuit

Additional Experiment-2

ZERO CROSSING DETECTOR

Aim: To design and setup a zero crossing detector circuit with OP AMP 741C and plot thewaveforms.

2.1 Apparatus:

Sl .No	Name and Specification	Quantity required
1	Dual power supply +/- 15V	1
2	Function generator (0- 1MHz)	1
3	Oscilloscope	1
4	Bread board	1
5	IC 741C	1
6	Probes and connecting wires	As required.

2.2 Theory:

It is the open loop/ saturation mode operation of op-amp. Here the signal is given thenon-inverting terminal. So the output signal is in phase with the input signal. Such a circuit iscalled non-inverting zero crossing detector. In open loop configuration, the gain of the opamp is very high, so when the input voltage is above zero voltage, output of the circuit goes to+ Vsat which is approximately +13V. Similarly when the input voltage is below zero voltage,the output goes to - Vsat which is approximately -13V.

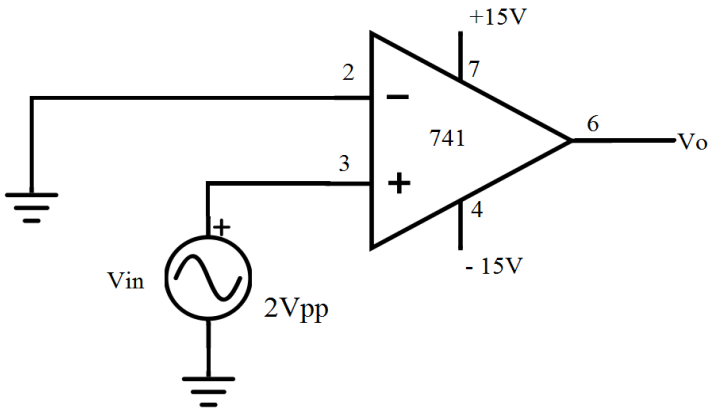

Fig 2.2 Zero crossing detector

Procedure:

1. Check the components.
2. Setup the circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Give Vin= 5 or 2V Vpp/ 1KHz sine wave.
5. Observe input and output on the oscilloscope simultaneously.
6. Note down and draw the input and output waveforms on the graph.
7. Verify the output.

Result:

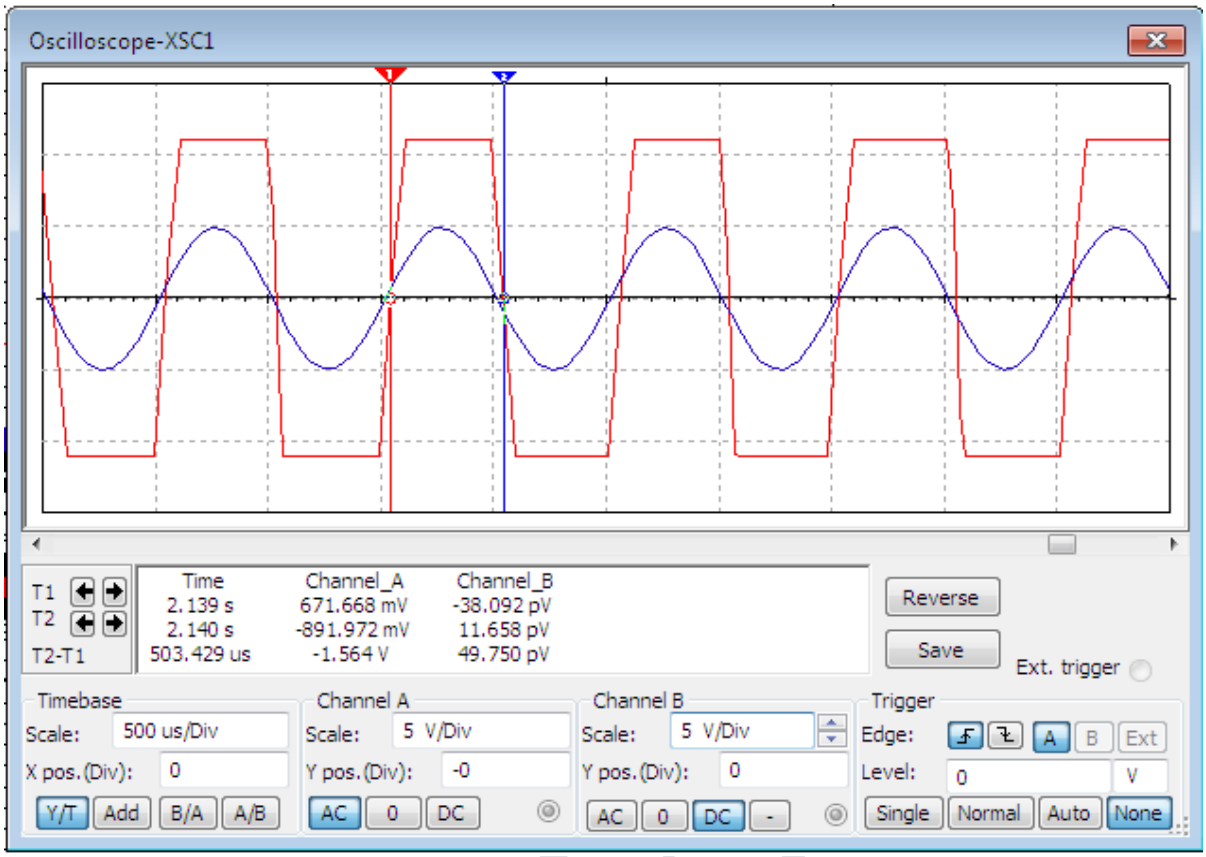

Fig 2.1: Zero crossing points of sinusoidal signal detected by zero crossing detector circuit

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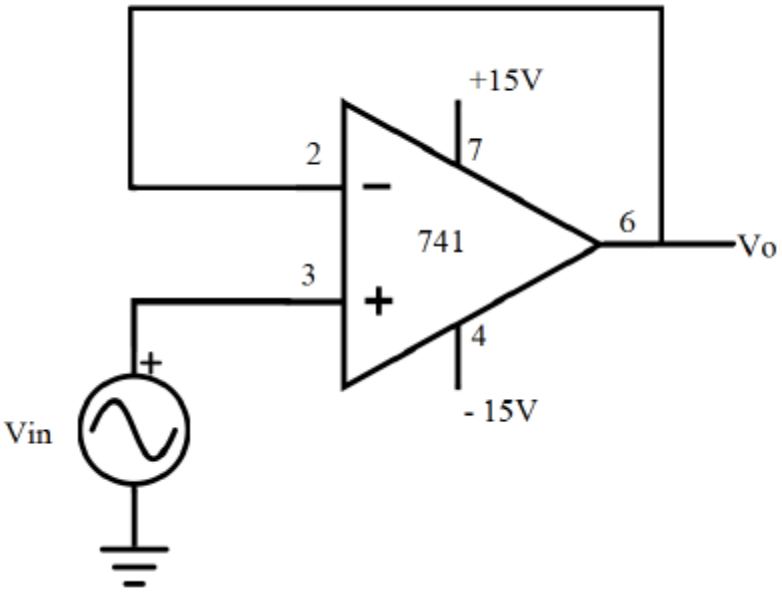
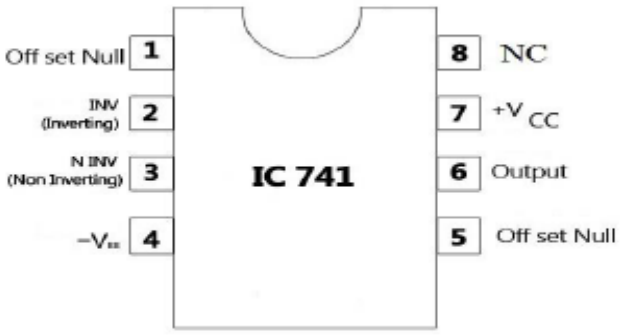


Fig 3.1 Circuit Diagram of voltage follower

741 pin diagram



Additional Experiment-2

VOLTAGE FOLLOWER

Aim: To design and setup a voltage follower circuit with OPAMP IC 741C and observe the waveforms.

3.1 Apparatus:

Sl. No	Name and Specification	Quantity required
1	Dual power supply +/- 15V	1
2	Function generator (0- 1MHz)	1
3	Oscilloscope	1
4	Bread board	1
5	IC 741C	1
6	Probes and connecting wires	As required.

Theory:

Principle:

A voltage follower (also called a unity-gain amplifier or buffer amplifier or isolationamplifier) is an op-amp circuit which has a voltage gain of 1. This means that the op ampdoes not provide any amplification to the signal. It is called a voltage follower because theoutput voltage follows the input voltage; means the output voltage is same as the inputvoltage. Though the gain is unity, this circuit offers high input impedance and low outputimpedance and hence it is used as buffer, which is used to isolate a low impedance load froma voltage source to eliminate any loading that might occur.

Procedure:

1.Check the components.

2. Setup the circuit on the breadboard and check the connections.

3. Switch on the power supply.

4. Give 2Vpp/ 1 KHz sine wave as input.

5. Observe input and output on the two channels of the oscilloscope simultaneously.

6. Note down and draw the input and output waveforms on the graph.

7. Verify that the input and output waveforms are same in magnitude and phase.

Design:

The voltage follower is a non-inverting amplifier with unity gain.

$A = 1 + R_f / R_i = 1$

Or $R_f / R_i = 0$

Therefore $R_f = 0$

Observation:

V_i = ?

Vo = ?

Phase difference between input and output waveforms = ?

Calculations

Voltage gain = Vo / Vi = ?

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